# Application Note :
# Telink Hardware Design Guide

AN-16101000-E1

**Ver 1.0.0**

**2016/10/14**

TELINK SEMICONDUCTOR



**Brief:**

This document is designed to provide developers with guide on Telink SoC-based hardware design.

It mainly introduces hardware functions and schematic design guide for TLSR8267/TLSR8267F512, TLSR8266/TLSR8266F512 and TLSR8263, as well as general PCB design rules.

**Published by**
**Telink Semiconductor**

**Bldg 3, 1500 Zuchongzhi Rd,**
**Zhangjiang Hi-Tech Park, Shanghai, China**



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For sales or technical support, please send email to the address of:

telinkcnsales@telink-semi.com

telinkcnsupport@telink-semi.com

## Revision History

| Version | Major Changes | Date | Author |
|---|---|---|---|
| 1.0.0 | Initial release | 2016/10 | W.W.X., Cynthia |

# Table of contents

# 1 Brief

This document is designed to provide developers with guide on Telink SoC-based hardware design. It mainly introduces hardware functions and schematic design guide for TLSR8267/TLSR8267F512, TLSR8266/TLSR8266F512 and TLSR8263, as well as general PCB design rules.

# 2 TLSR8267/TLSR8267F512 Hardware Design Guide

## 2.1 Hardware functions

| No. | Item | Description |
|---|---|---|
| 1 | Package | ✧ Both TLSR8267 and TLSR8267F512 support QFN32 and QFN48 package. |
| 2 | Program memory (Flash) | ✧ TLSR8267F512 embeds 512KB Flash.<br>✧ TLSR8267 supports external 128/512KB Flash. |
| 3 | Clock | ✧ For applications with requirement of accurate timing (e.g. electronic label), it's needed to connect external 32.768KHz crystal via the ANA_C<2> and ANA_C<3> pin. |
| 4 | Swire | Support Single Wire interface:<br>✧ TLSR8267 QFN32 package only supports SWS (Single Wire Slave).<br>✧ Other packages support both SWM (Single Wire Master) and SWS.<br>✧ When 8267 acts as Slave, it can communicate with SWM of Master via SWS.<br>✧ When 8267 acts as Master, it can communicate with SWS of Slave via SWM. |
| 5 | GPIO | ✧ TLSR8267F512 QFN32/QFN48 package supports up to 21/36 GPIOs.<br>✧ TLSR8267 QFN32/QFN48 package supports up to 21/37 GPIOs. |
| 6 | Wakeup source | ✧ ANA_A<0>~ANA_E<3> can be independently configured as active-high or active-low Pad wakeup sources. |
| 7 | Pull-up/Pull-down resistor | ✧ ANA_A<0>~ANA_E<3> support independently configurable 10KΩ/1MΩ pull-up resistor or 100KΩ pull-down resistor which are all disabled by default.<br>✧ The DP pin also supports configurable 1.5KΩ pull-up resistor for USB use. This pull-up resistor is disabled by default. |
| 8 | Driving strength (DS) | ✧ ANA_E<1>, ANA_E<0>: maximum=16mA ("DS"=1), minimum=12mA ("DS"=0).<br>✧ ANA_E<3>, ANA_E<2>: maximum=12mA ("DS"=1), minimum=8mA ("DS"=0).<br>✧ Other GPIO pins support maximum drive level of 4mA ("DS"=1) and minimum drive level of 0.7mA ("DS"=0)<br>✧ The "DS" configuration will take effect when the pin is used as output, and it's set as the strongest driving level by default. |

| No. | Item | Description |
|---|---|---|
| 9 | PWM | ✧ Support 6-channel PWM output: PWM0~PWM5. PWM#n_N indicates inverted output.<br>✧ PWM0~PWM5 all support continuous output mode.<br>✧ PWM0 and PWM1 support 3 modes including continuous mode, counting mode and IR mode. Other PWM channels only support continuous mode.<br>✧ Only PWM1/1_N and PWM0/0_N can be used as IR driving IOs. |
| 10 | I2C | ✧ Embed I2C hardware module.<br>✧ Support Master and Slave mode. Act as Slave mode by default.<br>✧ One group among ANA_A<3>/ANA_A<4>, ANA_B<6>/ANA_B<7> and ANA_C<0>/ANA_C<1> can be configured as SDA/SCL to communicate with other device via I2C. |
| 11 | SPI | ✧ Embed SPI hardware module.<br>✧ Support Master and Slave mode. Act as Slave mode by default.<br>✧ One group among ANA_A<2>~ANA_A<5> and ANA_B<4>~ANA_B<7> can be configured as SPI pins to communicate with other device via SPI. |
| 12 | I2C and SPI usage | I2C hardware and SPI hardware modules in the chip share part of the hardware, as a result, when both hardware interfaces are used, the restrictions listed below need to be taken into consideration.<br>✧ I2C and SPI hardware cannot be used as Slave at the same time.<br>✧ I2C Slave mode and SPI Master mode cannot be used at the same time.<br>✧ I2C Master mode and SPI Slave mode cannot be used at the same time.<br>✧ I2C and SPI can be used as Master at the same time only when ANA_A<2>~ ANA_A<5> are configured as SPI pins and ANA_C<0>~ ANA_C<1> are configured as I2C pins. Note that it's needed to configure related registers before each I2C/SPI operation. Please refer to corresponding SDK. |
| 13 | UART | ✧ Embed UART to implement full-duplex transmission and reception.<br>✧ One group among ANA_A<6>/ANA_A<7>, ANA_B<2>/ANA_B<3> and ANA_C<2>/ANA_C<3> can be configured as TX/RX to communicate with other device via UART.<br>✧ Support hardware flow control when ANA_C<4> and ANA_C<5> are configured as RTS and CTS pins. |
| 14 | Analog microphone (AMIC) | ✧ Support AMIC input.<br>✧ Adopt differential input by default: use ANA_C<3>/ANA_C<4>/ANA_C<5> as AmicBias/AmicSN/AmicSP.<br>✧ If PC3 is configured as other multiplexed function, other pin of PortC can be used as AmicBias. |

| No. | Item | Description |
|---|---|---|
| 15 | Digital microphone (DMIC) | ✧ Support DMIC input.<br>✧ Use ANA_A<0>/ANA_A<1> as DMIC_DI/DMIC_CLK. |
| 16 | Audio output (SDM) | ✧ Support mono-channel audio output.<br>✧ Use ANA_E<0>/ANA_E<1> as SDM_P/SDM_N. |
| 17 | ADC | ✧ ADC input channel: ANA_B<0>~ANA_B<7>, ANA_C<0>~ANA_C<1>, ANA_C<6>~ANA_C<7>. |
| 18 | Battery detect | ✧ For battery detect, the ANA_B<7> pin is used by default.<br>✧ If dual dry batteries are directly used to supply power, system power supply can be configured as reference voltage for internal ADC. The system voltage can be directly detected without the need of the PB7 pin of the chip.<br>✧ If single dry battery is used to supply power via boost DCDC, it's needed to directly connect the PB7 pin with the battery to detect its voltage. No external divider resistor is needed.<br>✧ If Li battery is used to supply power via LDO step-down circuit, to detect battery voltage, it's needed to connect the PB7 pin with the battery via external 2:1 divider resistors so that the PAD can bear the voltage. |

## 2.2 Schematic design guide

| No. | Item | Description |
|---|---|---|
| 1 | VDDDEC | ✧ VDDDEC should be connected to GND via 1uF filtering capacitor. |
| 2 | DVDD3F | ✧ DVDD3F should be connected to GND via 10uF filtering capacitor. |
| 3 | DVDD, AVDD | ✧ Both DVDD and AVDD pin should be connected with a 1uF decoupling capacitor. |
| 4 | Reset pin | ✧ RST pin should be connected to GND via 1uF capacitor. |
| 5 | Test points for FW burning and wakeup source | ✧ It's needed to reserve three test points including VCC, GND and SWS for firmware burning.<br>✧ According to test plan, it's needed to reserve a GPIO test point as wakeup source for sleep/wakeup test. It's recommended to use ANA_B<1> as wakeup source corresponding to Telink standard test script. |
| 6 | Crystal oscillator | ✧ It's recommended to use 12MHz crystal with spec of 12MHz-12pF-+/-20ppm.<br>✧ Load capacitors are reserved for crystal pins (not soldered by default). |
| 7 | BQB certificate<br>&<br>FCC RF certificate | ✧ It's needed to reserve TX/RX test points for BLE BQB certificate test.<br>✧ FCC RF certificate matching location: It's needed to reserve π-type low pass filtering circuit for ANT pin in order to decrease RF harmonic energy. Default parameters: 2.2nH series inductor, two 1.5pF shunt capacitors. |
| 8 | Antenna | ✧ Telink solution uses monopole PCB antenna.<br>✧ It's needed to reserve a shunt device matching location near the antenna port for antenna match debug. |
| 9 | USB | ✧ For USB dongle applications, it's needed to connect a 33Ω series resistor between the DP/DM pin and the USB port, and the resistor should be close to the USB port. |
| 10 | Power supply for MIC module | ✧ PIN28/PIN20 of TLSR8267F512 QFN48/QFN32 package supplies power for mic module. It's needed to adopt star-type connection, i.e. single power line is needed to trace from DVDD source to this pin. Pay special attention to this point on PCB design. |
| 11 | IR power supply | ✧ For remote control applications, it's needed to connect IR power supply to GND via 220uF/10V filtering capacitor. |

# 3 TLSR8266/TLSR8266F512 Hardware Design Guide

## 3.1 Hardware functions

| No. | Item | Description |
|---|---|---|
| 1 | Package | ✧ TLSR8266 supports QFN56, QFN48 and QFN32 package.<br>✧ TLSR8266F512 supports QFN48 and QFN32 package.<br>✧ TLSR8266F128 supports QFN24 package. |
| 2 | Program memory (Flash) | ✧ TLSR8266F512 embeds 512KB Flash.<br>✧ TLSR8266F128 embeds 128KB Flash.<br>✧ TLSR8266 supports external 128/512KB Flash. |
| 3 | Swire | Support Single Wire interface:<br>✧ QFN32 and QFN24 only support SWS (Single Wire Slave).<br>✧ Other packages support both SWM (Single Wire Master) and SWS.<br>✧ When 8266 acts as Slave, it can communicate with SWM of Master via SWS.<br>✧ When 8266 acts as Master, it can communicate with SWS of Slave via SWM. |
| 4 | GPIO | ✧ TLSR8266F512 QFN32/QFN48 package supports up to 20/35 GPIOs.<br>✧ TLSR8266 QFN32/QFN48/QFN56 package supports up to 22/37/41 GPIOs.<br>✧ TLSR8266F128 QFN24 package supports up to 12 GPIOs. |
| 5 | Wakeup source | ✧ ANA_A<0>~ANA_F<1> can be independently configured as active-high or active-low Pad wakeup sources.<br>✧ It's not recommended to use ANA_C<0>~ANA_C<3> as wakeup pins. |
| 6 | Pull-up/Pull-down resistor | ✧ All GPIOs support independently configurable 10KΩ/1MΩ pull-up resistor or 100KΩ pull-down resistor which are all disabled by default.<br>✧ The DP pin also supports configurable 1.5KΩ pull-up resistor (disabled by default). To enable this pull-up resistor, set analog register 0x00[4] as 1. |
| 7 | DM/DP | ✧ When GPIO function is enabled, the DM and DP pin can only be used as GPI (input). |
| 8 | Driving strength (DS) | ✧ ANA_B<6>, ANA_B<5>: maximum=8mA ("DS"=1), minimum=4mA ("DS"=0).<br>✧ ANA_E<5>, ANA_E<4>: maximum=16mA ("DS"=1), minimum=12mA ("DS"=0).<br>✧ Other GPIO pins support maximum drive level of 4mA ("DS"=1) and minimum drive level of 0.7mA ("DS"=0).<br>✧ The "DS" configuration will take effect when the pin is used as output, and it's set as the strongest driving level by default. |

| No. | Item | Description |
|---|---|---|
| 9 | GPIO default state | ✧ GPIO acts as input by default except ANA_B<0> and ANA_D<5:4>: ANA_B<0> and ANA_D<4> output 1, while ANA_D<5> outputs 0. |
| 10 | PWM | ✧ Supports 6-channel PWM output: PWM0~PWM5. PWM#n_N indicates inverted output.<br>✧ PWM0~PWM5 all support continuous output mode.<br>✧ PWM0 and PWM1 support 3 modes including continuous mode, counting mode and IR mode. Other PWM channels only support continuous mode.<br>✧ Only PWM1/1_N and PWM0/0_N can be used as IR driving IOs. |
| 11 | I2C | ✧ Embed I2C hardware module.<br>✧ Support Master and Slave mode. Act as Slave mode by default.<br>✧ ANA_E<7>/ANA_F<1> can be configured as SDA/SCL to communicate with other device via I2C. |
| 12 | SPI | ✧ Embed SPI hardware module.<br>✧ Support Master and Slave mode. Act as Slave mode by default.<br>✧ ANA_E<6>/ANA_E<7>/ANA_F<0>/ANA_F<1> can be configured as SPI CN/DI/DO/CK pins to communicate with other device via SPI. |
| 13 | I2C and SPI usage | I2C hardware and SPI hardware modules in the chip share part of the hardware, as a result, when both hardware interfaces are used, the restrictions listed below need to be taken into consideration.<br>✧ I2C and SPI hardware cannot be used as Slave at the same time.<br>✧ I2C Slave mode and SPI Master mode cannot be used at the same time.<br>✧ I2C Master mode and SPI Slave mode cannot be used at the same time.<br>✧ I2C and SPI can be used as Master at the same time only when specific GPIO pins are configured as I2C and SPI pins, respectively. Please refer to corresponding SDK. |
| 14 | UART | ✧ Embed UART to implement full-duplex transmission and reception.<br>✧ ANA_C<6>/ANA_C<7> can be configured as TX/RX to communicate with other device via UART.<br>✧ Support hardware flow control when ANA_D<0>/ANA_D<1> or ANA_E<6>/ANA_F<0> are configured as RTS and CTS pins. |
| 15 | Analog microphone (AMIC) | ✧ Support AMIC input.<br>✧ Adopt single-end input: use ANA_C<0>/ANA_C<1> as AmicBias/AmicIn. |
| 16 | Digital microphone (DMIC) | ✧ Support DMIC input.<br>✧ Use ANA_E<1>/ANA_E<2> as DMIC_CLK/DMIC_DI. |

| No. | Item | Description |
|---|---|---|
| 17 | Audio output (SDM) | ✧ Support mono-channel audio output.<br>✧ Use ANA_E<4>/ANA_E<5> as SDM_P/SDM_N. |
| 18 | ADC | ✧ ADC input channel: ANA_C<2>~ANA_C<7>, ANA_D<0>~ANA_D<5>. |
| 19 | Battery detect | ✧ It's needed to use one ADC input channel to detect battery voltage.<br>✧ It's needed to connect external divider resistor for all power supply methods. |
| 20 | TLSR8266F512 pin connection | For TLSR8266F512 QFN32 package, it's needed to connect PIN3 with PIN8.<br>For TLSR8266F512 QFN48 package, it's needed to connect PIN3 with PIN12. |

## 3.2 Schematic design guide

| No. | Item | Description |
|---|---|---|
| 1 | VDDDEC | ✧ VDDDEC should be connected to GND via 1uF filtering capacitor. |
| 2 | DVDD，AVDD | ✧ Both DVDD and AVDD pin should be connected with a 1uF decoupling capacitor. |
| 3 | Reset pin | ✧ RST pin should be connected to GND via 1uF capacitor. |
| 4 | Crystal oscillator | ✧ It's recommended to use 12MHz crystal with spec of 12MHz-12pF-+/-20ppm.<br>✧ Load capacitors are reserved for crystal pins (not soldered by default). |
| 5 | Test points for FW burning and wakeup source | ✧ It's needed to reserve three test points including VCC, GND and SWS for firmware burning.<br>✧ According to test plan, it's needed to reserve a GPIO test point as wakeup source for sleep/wakeup test. It's recommended to use ANA_C<2> as wakeup source corresponding to Telink standard test script. |
| 6 | BQB certificate<br>&<br>FCC RF certificate | ✧ It's needed to reserve TX/RX test points for BLE BQB certificate test.<br>✧ FCC RF certificate matching location: It's needed to reserve π-type low pass filtering circuit for ANT pin in order to decrease RF harmonic energy. Default parameters: 2.2nH series inductor, two 1.5pF shunt capacitors. |
| 7 | Antenna | ✧ Telink solution uses monopole PCB antenna.<br>✧ It's needed to reserve a shunt device matching location near the antenna port for antenna match debug. |
| 8 | Does default state of PB0/PD4/PD5 influence circuit? | ✧ By default ANA_B<0> and ANA_D<4> output high level, and ANA_D<5> outputs low level. If any of the three IOs is used in circuit design, please take its default state into consideration. |
| 9 | USB | ✧ For USB dongle applications, it's needed to connect a 33Ω series resistor between the DP/DM pin and the USB port, and the resistor should be close to the USB port. |
| 10 | TLSR8266F512/F128 power supply | ✧ For TLSR8266F512/F128, its internal Flash won't work if its power supply drops below 2.7V.<br>✧ Consider using Li battery or four AAA dry batteries, and then use LDO step-down circuit to supply power for system.<br>✧ If Li battery is used, please reserve system reset circuit for miniUSB interface. |

# 4 TLSR8263 Hardware Design Guide

## 4.1 Hardware functions

| No. | Item | Description |
|---|---|---|
| 1 | Package | ✧ Support QFN24, TSSOP16 and ESOP8L package. |
| 2 | Program memory (OTP/Flash) | ✧ Embed 16KB OTP.<br>✧ TLSR8263ET24 supports external 128/512KB Flash. |
| 3 | Swire | ✧ Support Single Wire Slave (SWS) interface.<br>✧ 8263 (Slave) can communicate with SWM of Master via SWS. |
| 4 | GPIO | ✧ TLSR8263ET24 supports up to 14 GPIOs.<br>✧ TLSR8236ES16 supports up to 9 GPIOs.<br>✧ TLSR8263EP8 supports up to 3 GPIOs.<br>✧ All digital IOs (including MSDO/MSDI/MSCN/MSCK) can be configured as GPIOs. |
| 5 | Wakeup source | 1. TLSR8263ET24:<br>✧ GP17~GP18, GP22~GP23 and GP31 can be configured as active-high or active-low Pad wakeup sources.<br>✧ GP17~GP18 wakeup polarity is configured at the same time.<br>✧ Wakeup polarity of GP22~GP23 and GP31 is independently configurable.<br><br>2. TLSR8263ES16:<br>✧ GP17~GP18 and GP22~GP23 can be configured as active-high or active-low Pad wakeup sources.<br>✧ GP17~GP18 wakeup polarity is configured at the same time.<br>✧ Wakeup polarity of GP22~GP23 is independently configurable.<br><br>3. TLSR8263EP8:<br>✧ GP17 can be configured as active-high or active-low Pad wakeup source. |
| 6 | Pull-up/Pull-down resistor | 1. TLSR8263ET24:<br>✧ GP17~GP18, GP22~GP23 and GP31 support independently configurable 10KΩ/1MΩ pull-up resistor or 100KΩ pull-down resistor.<br>✧ GP5 and GP9~GP10 support independently configurable 100KΩ pull-down resistor.<br>✧ By default the pull-up and pull-down resistors are disabled.<br><br>2. TLSR8263ES16:<br>✧ GP17~GP18 and GP22~GP23 support independently configurable 10KΩ/1MΩ pull-up resistor or 100KΩ pull-down resistor.<br>✧ GP4~GP5, GP7 and GP10 support independently configurable 100KΩ |

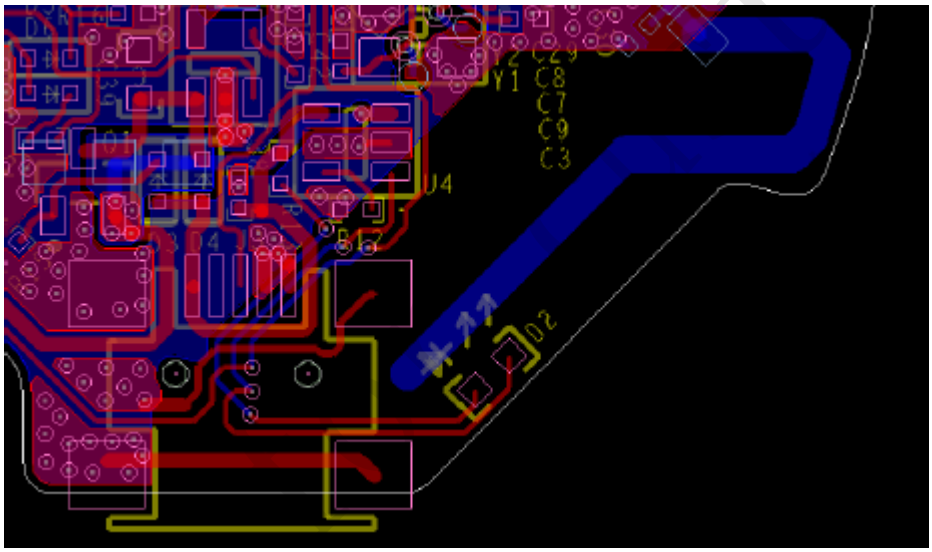
| No. | Item | Description |
|---|---|---|
| | | pull-down resistor.<br>✧ By default the pull-up and pull-down resistors are disabled.<br><br>3. TLSR8263EP8:<br>✧ GP17 supports configurable 10KΩ/1MΩ pull-up resistor or 100KΩ pull-down resistor.<br>✧ GP5 supports configurable 100KΩ pull-down resistor. |
| 7 | Driving strength (DS) | ✧ MCLK/MSDO/MSDI/MSCN: maximum=4mA (“DS”=1), minimum=2mA (“DS”=0).<br>✧ SWS: maximum=8mA (“DS”=1), minimum=4mA (“DS”=0).<br>✧ Other GPIO pins support maximum drive level of 4mA (“DS”=1) and minimum drive level of 0.7mA (“DS”=0).<br>✧ The “DS” configuration will take effect when the pin is used as output, and it’s set as the strongest driving level by default. |
| 8 | PWM | ✧ Support 4-channel PWM output: PWM0~PWM3. PWM#n_INV indicates inverted output.<br>✧ PWM0 supports two modes: continuous mode, counting mode.<br>✧ PWM1~PWM3 only support continuous mode.<br>✧ IR driving is not supported. |
| 9 | I2C | ✧ Embed I2C hardware module.<br>✧ Only support Slave mode. SCL should be configured as input.<br><br>1. TLSR8263ET24:<br>✧ GP22/GP23 can be configured as SCL/SDA, and internal 10KΩ pull-up resistor can be used.<br>✧ GP30/PG31 can be configured as SCL/SDA, and it’s needed to connect external pull-up resistor.<br>✧ GP5 can’t be configured as SDA.<br><br>2. TLSR8263ES16：<br>✧ GP4/GP5 can be configured as SCL/SDA, and it’s needed to connect external pull-up resistor.<br>✧ GP22/GP23 can be configured as SCL/SDA, and internal 10KΩ pull-up resistor can be used.<br><br>3. TLSR8263EP8 does not support I2C interface. |
| 10 | ADC | ✧ Support 4 ADC input channels via G17/G18/G22/G23 pin.<br>✧ Except for G23 with internal divider resistors, other ADC input pin should be connected with external 1/3 divider resistors. |

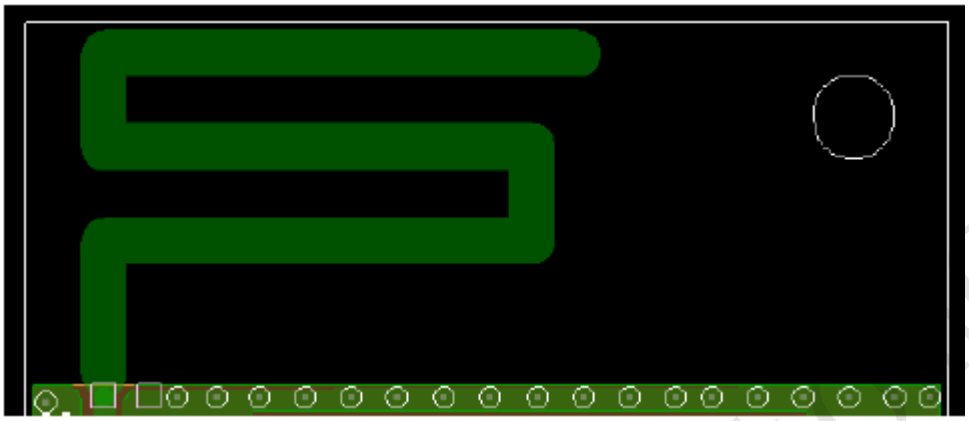
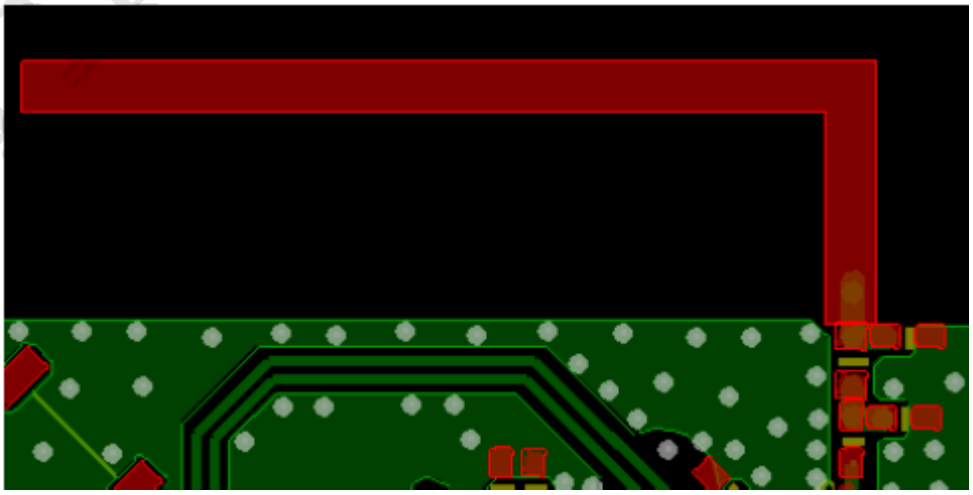
| No. | Item | Description |
|---|---|---|
| 11 | Battery detect | Use G23 with internal 1/3 divider resistors as battery detect pin, so that no external divider resistors are needed. |

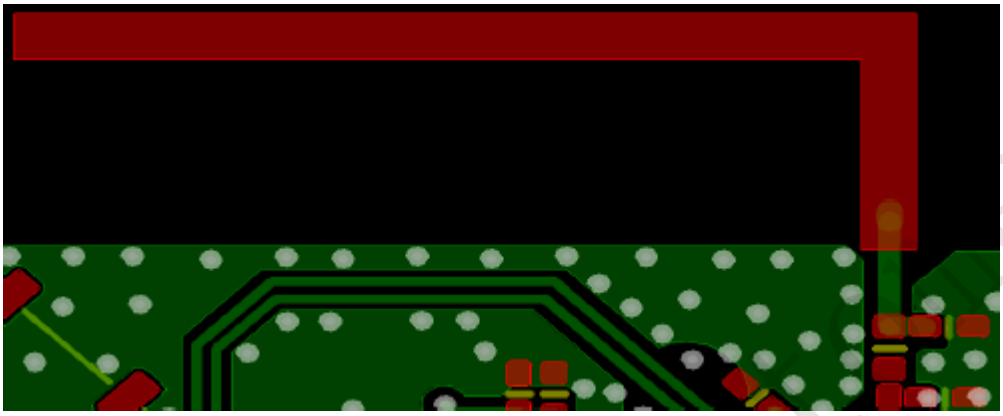
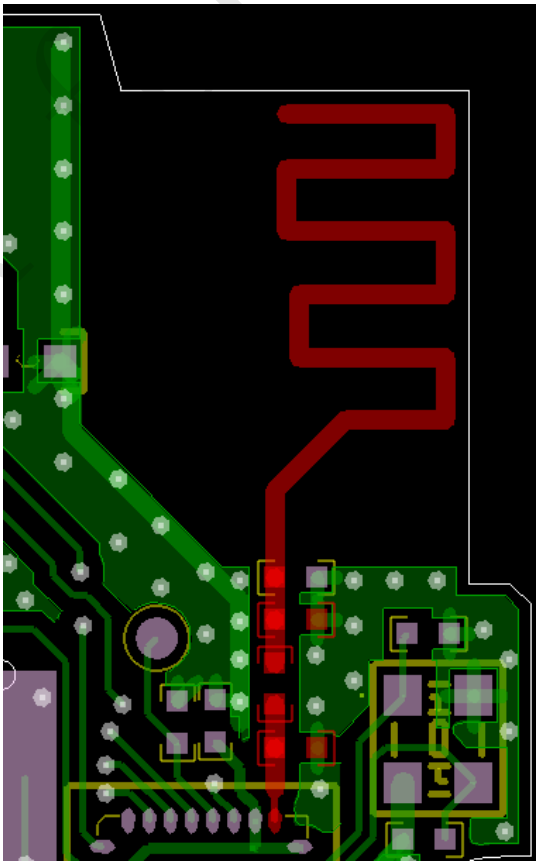
## 4.2 Schematic design guide

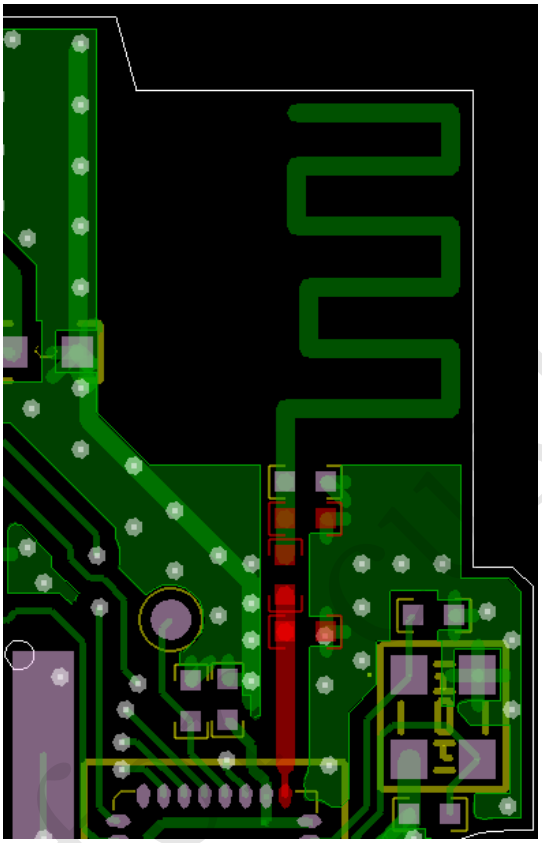
| No. | Item | Description |
|---|---|---|
| 1 | VDDDEC | ✧ VDDDEC should be connected to GND via 1uF filtering capacitor. |
| 2 | DVDD, AVDD | ✧ Both DVDD and AVDD pin should be connected with a 1uF decoupling capacitor. |
| 3 | Reset pin | ✧ RST pin should be connected to GND via 1uF capacitor. |
| 4 | Test points for FW burning and wakeup source | ✧ It's needed to reserve four test points including VCC, GND, SWS and VPP for OTP burning.<br>✧ According to test plan, it's needed to reserve a GPIO test point as wakeup source for sleep/wakeup test. It's recommended to use GP17 as wakeup source corresponding to Telink standard test script. |
| 5 | BQB certificate<br>&<br>FCC RF certificate | ✧ It's needed to reserve three test points including SDA, SCL and one GPIO for BLE BQB certificate test.<br>✧ FCC RF certificate matching location: It's needed to reserve π-type low pass filtering circuit for ANT pin in order to decrease RF harmonic energy. Default parameters: 2.2nH series inductor, two 1.5pF shunt capacitors. |
| 6 | Antenna | ✧ Telink solution uses monopole PCB antenna.<br>✧ It's needed to reserve a shunt device matching location near the antenna port for antenna match debug. |
| 7 | ROW/COL | For remote control applications:<br>✧ ROW pins should be selected as IOs with internal pull-up resistor.<br>✧ COL pins should be selected as IOs with internal pull-down resistor.<br>✧ If COL pins are selected as MSDO/MSDI/MSCN/MCLK, it's needed to connect external 100K pull-down resistor. |
| 8 | EEPROM | ✧ In remote control applications, OTP is used for burning, and EEPROM should be reserved to store user information. |
| 9 | Battery detect | ✧ Use G23 as battery detect pin, and no external divider resistors are needed for 3V power supply. |
| 10 | VPP | ✧ VPP should be supplied with external 6.75V power for OTP burning. |

# 5 General PCB Design Rules

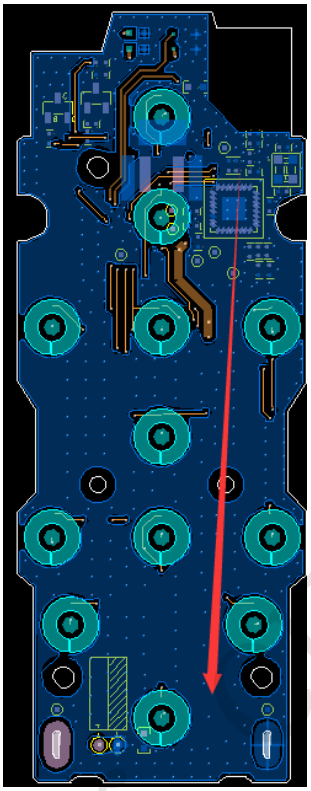
| No. | General PCB design rules |
|---|---|
| 1 | ✧ Decoupling capacitors of chip power pins should be placed close to the power pins. |
| 2 | ✧ Filtering capacitors of VDDDEC and DVDD3F should be placed close to the VDDDEC and DVDD3F pin. |
| 3 | ✧ Keep the antenna 5mm (or above) away from metal devices (e.g. metal screw, metal board frame).<br>✧ The figure below shows a bad design example: Antenna design is close to USB connector.<br>  |
| 4 | ✧ Since battery would largely influence antenna Tx/Rx performance, keep the antenna 3~5mm (or above) away from the battery. |
| 5 | ✧ Antenna trace width shouldn't be too narrow in order to decrease loss; line width should be 0.5mm or above, generally it's recommended to be 0.5mm or 1mm. |
| 6 | ✧ Top and bottom of antenna location should not be covered by GND.<br>✧ The distance between antenna and GND should be 3mm or above. |
| 7 | ✧ Generally antenna length is 20~40mm. The smaller the GND is, the longer the antenna should be. |
| 8 | ✧ There should be a row of via holes along the antenna on the side parallel to GND.<br>✧ Do not directly expose trace or pad to the antenna.<br>✧ The figure below shows a good design example: Via holes are placed evenly. |

| No. | General PCB design rules |
|---|---|
| |  <br>✧ The figure below shows a bad design example: Trace is directly exposed to the antenna, and the GND connection is not good.<br>  |
| 9 | ✧ Antenna matching components should be placed at the boundary of antenna and GND without shrink inward or expand outward.<br>✧ The figure below shows a good design example: Matching components are placed at the boundary of the antenna and GND.<br>  |

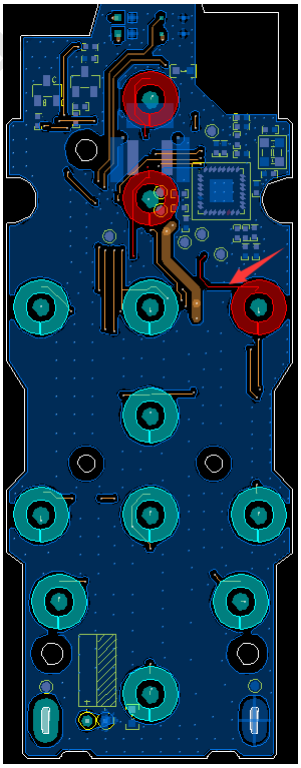
| No. | General PCB design rules |
|---|---|
| | ✧ The figure below shows a bad design example: Matching components shrink inward the GND.<br>  |
| 10 | ✧ Place the π-type filtering device of RF close to the RF pin.<br>✧ The RF line to the antenna port should be short. If the RF line is not short enough, it must be designed as 50ohm micro-strip line.<br>✧ There should be even via holes along the RF line, and the ground plane should be integral.<br>✧ The figure below shows a good design example: The π-type filtering device is placed close to the RF pin.<br>  |

| No. | General PCB design rules |
|---|---|
| | ✧ The figure below shows a bad design example: The π-type filtering device is placed away from the RF pin.<br>  |
| 11 | ✧ Power line should be as thick and short as possible.<br>✧ Generally width of power line is 0.5mm~0.6mm.<br>✧ If power line is not short enough, consider using 0.8mm (or above) width. |
| 12 | ✧ Ground current should have wide and fluent loopback path from RF GND to chip GND, then to power GND. Try to keep the integrity of ground plane.<br>✧ The figure below shows a good design example: Loopback path is wide from RF GND to chip GND then to battery GND. |

| No. | General PCB design rules |
|---|---|



✧ The figure below shows a bad design example: Loopback path from chip GND to battery GND is cut off by signal line.



| No. | General PCB design rules |
|---|---|
| 13 | ✧ Ground loopback should return to battery after filtered by LDO capacitor. |
| 14 | ✧ To avoid mutual interference, modules such as crystal oscillator, Audio, Mic and USB should be isolated with GND and protected by via holes as much as possible. |
| 15 | ✧ For modules such as Audio, Mic and USB, it's better to keep the integrity of ground plane without division. |
| 16 | ✧ For audio applications, it's needed to adopt star-type connection for power in order to decrease noise caused by dirty power. |