Assembly And Maintenance Manual for

Telink BLE 1x6 Test System 3.2

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Keyword

BLE, Assembly, Maintenance Manual

Brief

This document is the assembly and maintenance guide for Telink BLE 1x6 Test System 3.2, and presents DUT examples with flash or OTP.

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Revision History

Version	Change Description
V1.0.0	Initial release.
V1.1.0	Removed chapters 3, 4, 5, and appendix 1

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1. Overall Architecture of 1x6 Test System 3.2

Telink BLE 1x6 Test System 3.2 consists of test bench and mechanical structure. The test bench includes hardware platform and firmware folder, and it's provided by Telink; while customer needs to make the mechanical structure suitable for DUT (Device Under Test), and connect cables according to the guide in this document.

A set of Test Bench mainly contains the following hardware resources.

1) A main Board provided by Telink. Figure 1-1 shows the correct direction to place the main board.

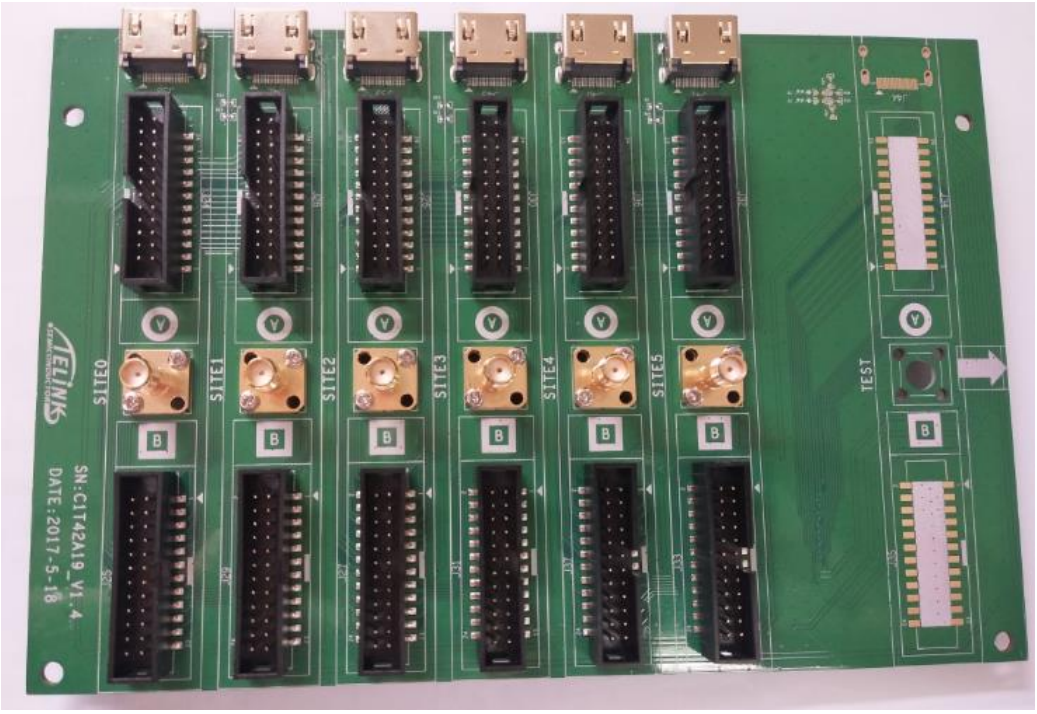

Figure 1-1 Top view of main board

2) Six EVK daughter boards provided by Telink. Each should be burned with the EVK firmware for test bench.

Figure 1-2 EVK daughter board

3) A Power board provided by Telink. It's pin-to-pin compatible with EVK daughter board and serves to supply power for test system.

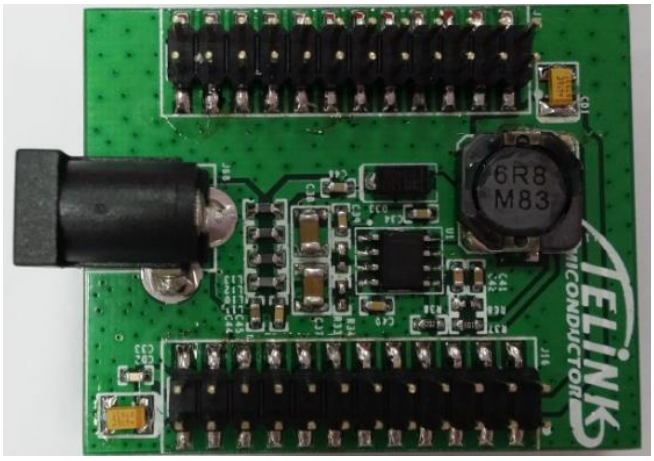

Figure 1-3 Power board

4) A display board provided by Telink. Its top side contains six groups of LEDs and six independent start buttons, while the bottom side contains six connectors.

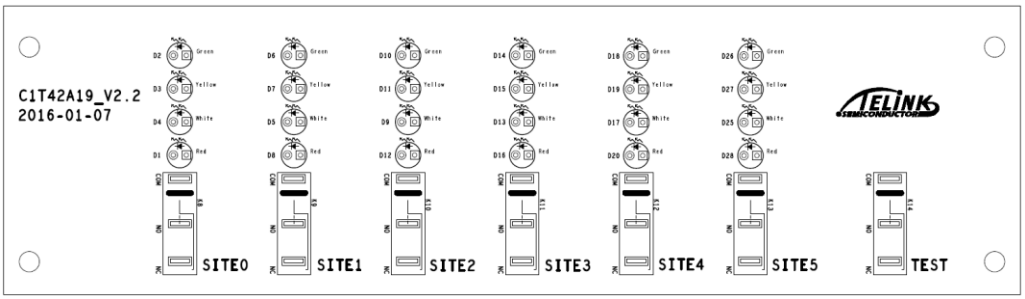

Figure 1-4 Top view

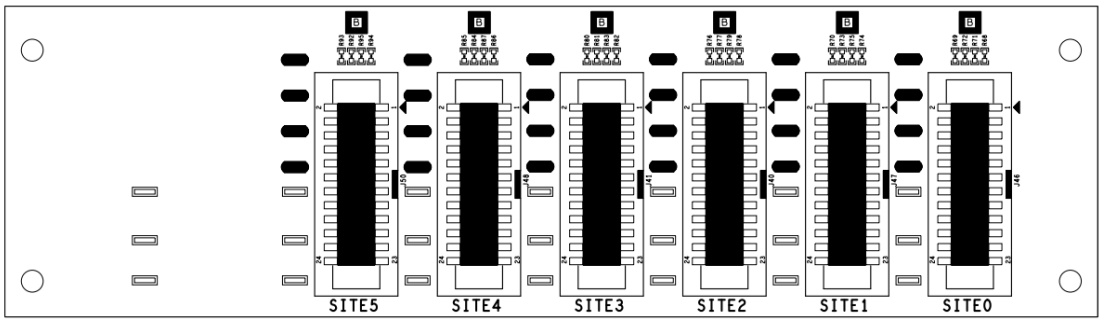

Figure 1-5 Bottom view

5) Six thimble boards. Each contains a HDMI connector and soldering points, so that each test site of main board can be connected with a DUT via a thimble board. Figure 1-6 shows an example of thimble board.

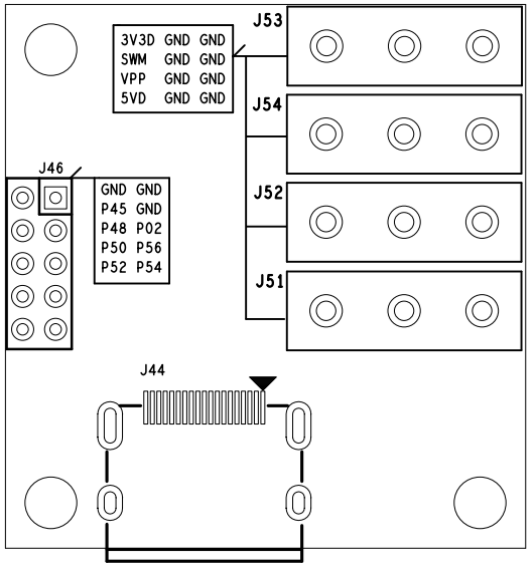

Figure 1-6 Thimble board

6) Six PCB Antenna boards and six RF cables provided by Telink, as shown in Figure 1-7.

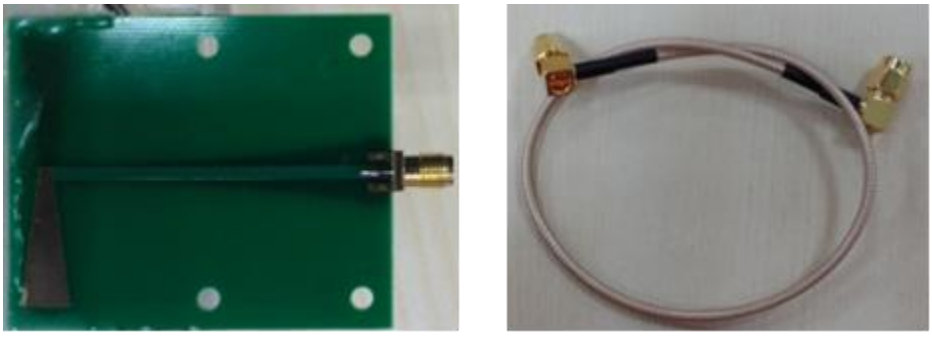

Figure 1-7 PCB antenna board and RF cable

7) A USB hub and six customized USB cables: The USB hub is used to connect six EVK daughter boards and PC.

8) A PC. On PC side, the EvkMonitor tool can be used to burn firmware for EVK daughter boards, and user can also observe test result via the EvkMonitor.

9) Six buzzer modules (Dimension: 50.2x16mm): Each is connected with a thimble board via a rainbow cable, thus it's connected to corresponding GPIO and Power of an EVK daughter board via HDMI interface of thimble board. The buzzer modules are used for Amic test.

   Each buzzer board should be placed as close to corresponding Amic as possible. Do not contact buzzer board with Amic directly, and there should be no obstacle between them.

Note

Buzzer boards are only supplied for DUT with MIC and not contained in the hardware resources by default.

Figure 1-8 Buzzer module

Six EVK daughter boards and Power board are directly connected with corresponding connectors on the bottom side of the main board (refer to **Section 2.2**).

Figure below shows the system connection chart.

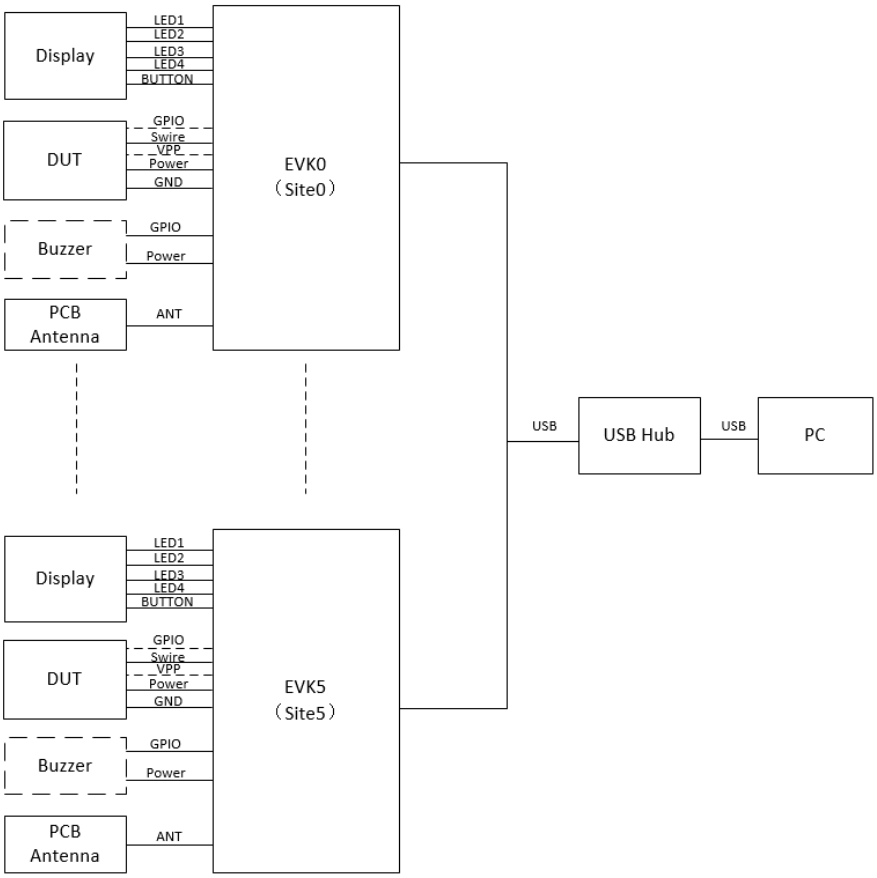

Figure 1-9 System connection chart

2. Hardware Platform Building

2.1 Check External Antenna

Telink test bench adopts external antennas for RF test. Customer needs to check the consistency of antennas. Figure 2-1 shows the PCB antenna supplied by Telink.

Figure 2-1 Telink PCB antenna board

Customer needs to make sliding blocks (as shown in Figure 2-2) which can fix the PCB antennas. The sliding blocks are used for distance debugging between the PCB antennas and PCBAs (DUTs) to guarantee test result consistency.

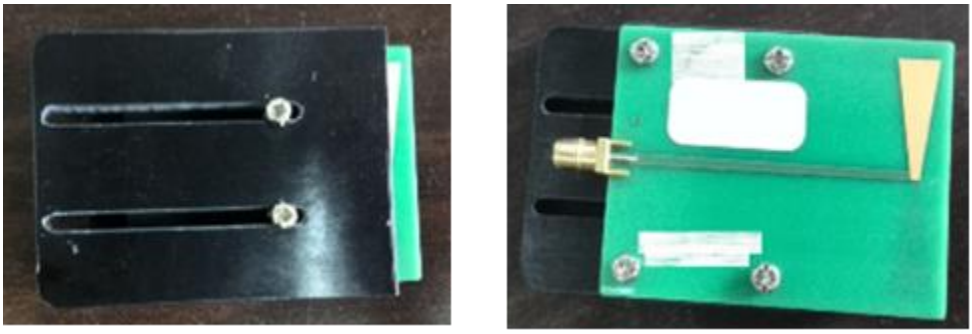

Figure 2-2 Sliding block to fix PCB antenna

Figure 2-3 shows dimensions in mm of the PCB antenna supplied by Telink.

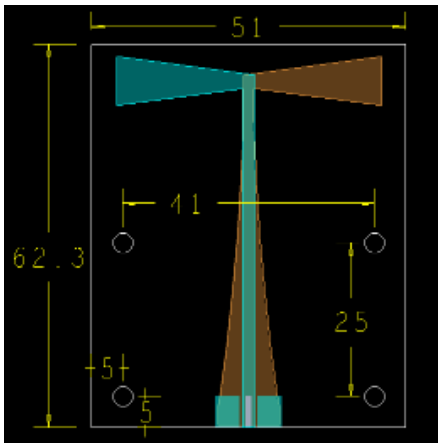

Figure 2-3 Telink PCB antenna dimensions

2.2 Hardware Assembly

Connect six EVK daughter boards (EVK0~EVK5) and Power board with corresponding connector location on the bottom side of the main board, as shown in Figure 2-5.

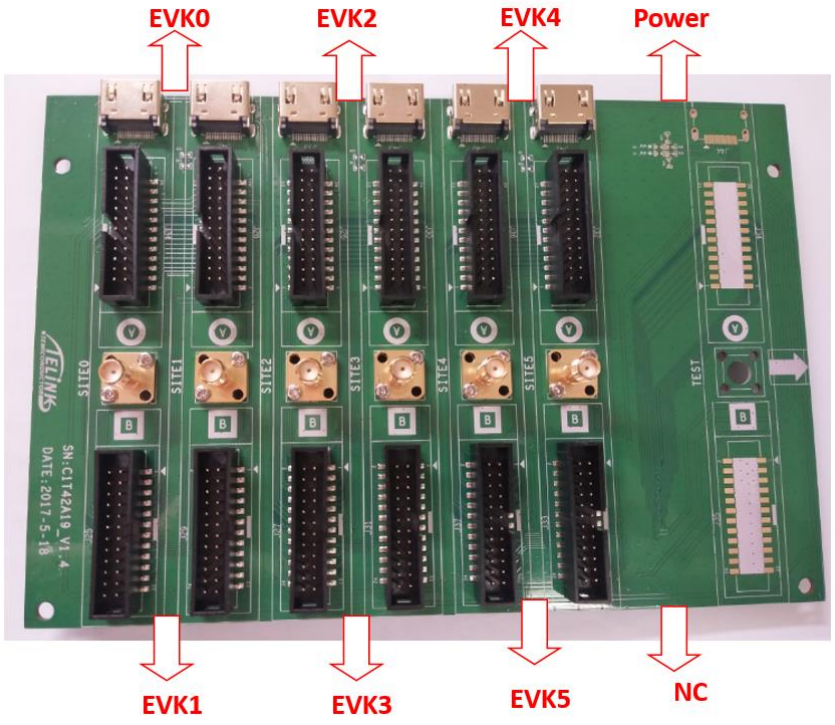

Figure 2-4 Top view of main board

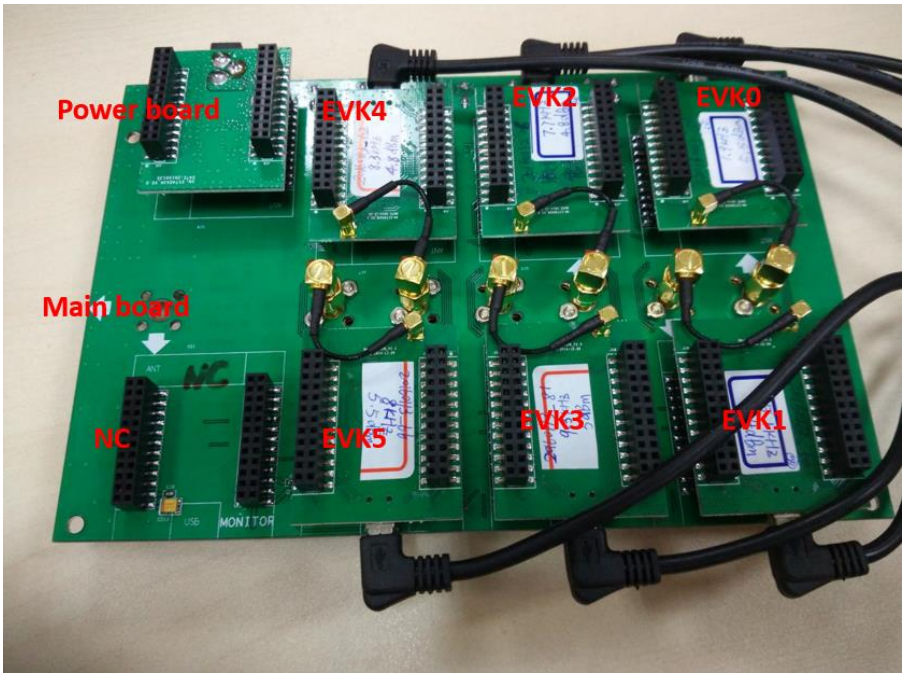

Figure 2-5 Assembly chart on the bottom side of main board

Note that USB interfaces of the EVK daughter boards, as well as power interface of the Power board should be placed towards the outside direction of the main board.

2.3 Cable Connection

2.3.1 Test Sites on Main Board

As shown in Figure 2-6, the top side of the main board contains six independent test sites (marked as Site0~Site5 from left to right). Note that the arrow should be placed towards right.

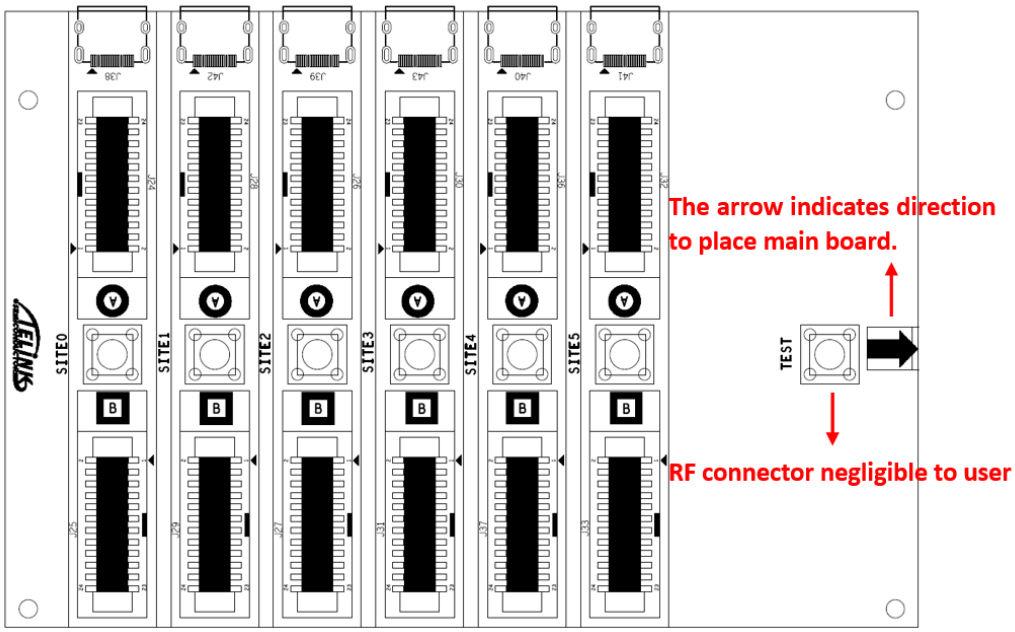

Figure 2-6 Top silk-screen sketch of main board

Each Site on the main board contains HDMI connector, connector A, flange plate and connector B from top to bottom. Connector A and B are featured with dual rows, 2.54mm spacing and 2x12pin.

Telink adopts a HDMI cable to connect a thimble board with HDMI connector on corresponding test site of the main board, and adopts a gray flat cable to connect a display board with corresponding connector B of the main board.

Please refer to **Appendix 2** for illustration of test pins on the main board.

2.3.2 Test Sites on Display Board

As shown in Figure 2-7, the bottom side of the display board contains six independent test sites (marked as Site5~Site0 from left to right).

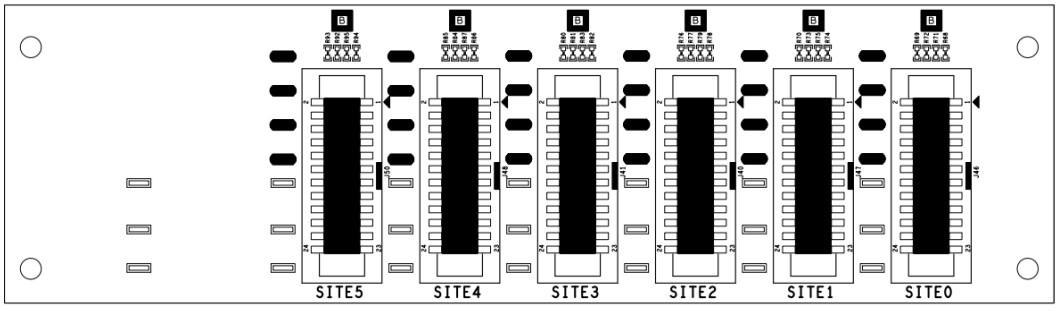

Figure 2-7 Bottom silk-screen of display board

Each site (e.g. Site0 in Figure 2-8) on the display board contains a mistake-proof connector (marked as B) featured with dual rows, 2.54mm spacing and 2x12pin.

In Figure 2-8, Site0 is taken as an example to show the mark of connection points on each test site of the display board. G, W, R, Y and Button indicate connection point Green-LED, White-LED, Red-LED, Yellow-LED, independent start button, respectively.

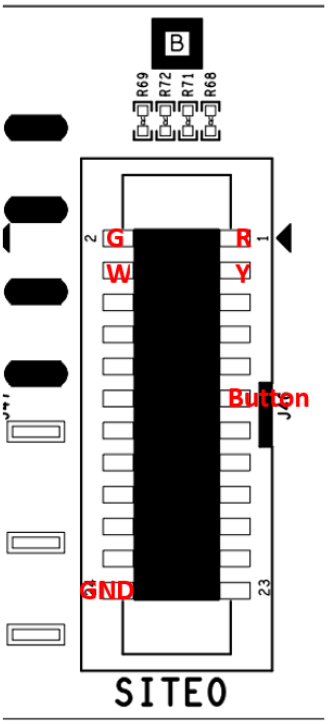

Figure 2-8 Connection points on test site of display board

2.3.3 Cable Connection Between Main Board and DUT Thimble

Telink provides six HDMI cables. HDMI connector on each test site of the main board should be connected with a thimble board's HDMI connector via a HDMI cable.

If DUT is a device board with flash, up to four cables should be connected between a thimble board and a DUT.

Table 2-1 Cable connection between thimble board and DUT with flash

Connection points on thimble board	Connection points on DUT
3V3D	BAT+

GND	BAT-
SWM	SWS
P45*	Wakeup GPIO*

***Note**

Wakeup test supports two methods including timer wakeup and GPIO wakeup.

- *If using timer wakeup, it's not needed to connect P45 of thimble board with DUT's wakeup GPIO.*
- *If using GPIO wakeup, it's needed to connect P45 of thimble board with DUT's wakeup GPIO.*

If DUT is a device board with OTP, up to five cables should be connected between a thimble board and a DUT.

Table 2-2 Cable connection between thimble board and DUT with OTP

Connection points on thimble board	Connection points on DUT
3V3D	BAT+
GND	BAT-
SWM	SWS
P45*	Wakeup GPIO*
VPP	VPP

***Note**

Wakeup test supports two methods including timer wakeup and GPIO wakeup.

- *If using timer wakeup, it's not needed to connect P45 of thimble board with DUT's wakeup GPIO.*
- *If using GPIO wakeup, it's needed to connect P45 of thimble board with DUT's wakeup GPIO.*

Note

To avoid ambient interference, all connection cables between thimble board and DUT should use STP (Shielded Twisted Pair) cable. Figure 2-9 shows cable connection chart.

2.3.4 Cable Connection Between Buzzer Board and Thimble Board

Each thimble board (connection points: P48, 3V3D, GND) should be connected with corresponding buzzer board (connection points: VCC, 3V3B, GND) via a 3P rainbow cable (Rainbow cable is supplied by Telink, and user can cut it as needed). Figure 2-9 shows cable connection chart.

Note

Buzzer boards are only supplied for DUT with MIC and not contained in the hardware resources by default.

2.3.5 Cable Connection Between Main Board and Display Board

Telink provides six gray flat cables. Connector B on each test site of the main board (connection points: Green-LED, Red-LED, White-LED, Yellow-LED, Button (Independent start button), GND) should be connected with connector B on corresponding Site of the display board (connection points: G, R, W, Y, Button, GND) via a gray flat cable. Figure 2-9 shows cable connection chart.

2.3.6 Cable Connection Between Main Board and PCB Antenna Board

Flange plate (SMA) on each test site of the main board should be connected with corresponding external PCB antenna board via a RF cable. Figure 2-9 shows cable connection chart.

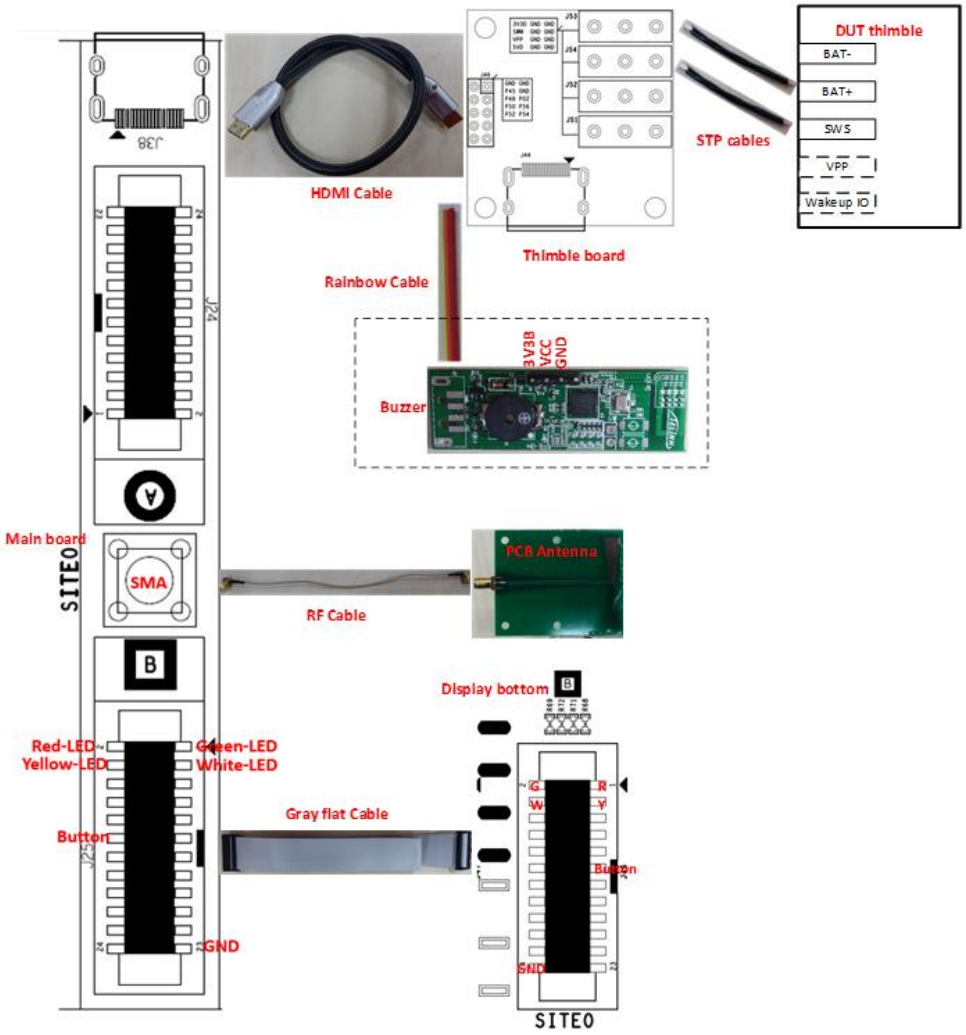

Figure 2-9 Cable connection chart

2.3.7 Other Cable Connection

The Power board should be connected with power to supply power for test system.

Each EVK daughter board should be connected with an USB interface of USB hub via an USB cable. The USB hub should be connected with PC via an USB cable. User can burn firmware for EVK daughter boards and observe test result via the EvkMonitor tool on PC side.

Figure 2-10 1x6 test system 3.2

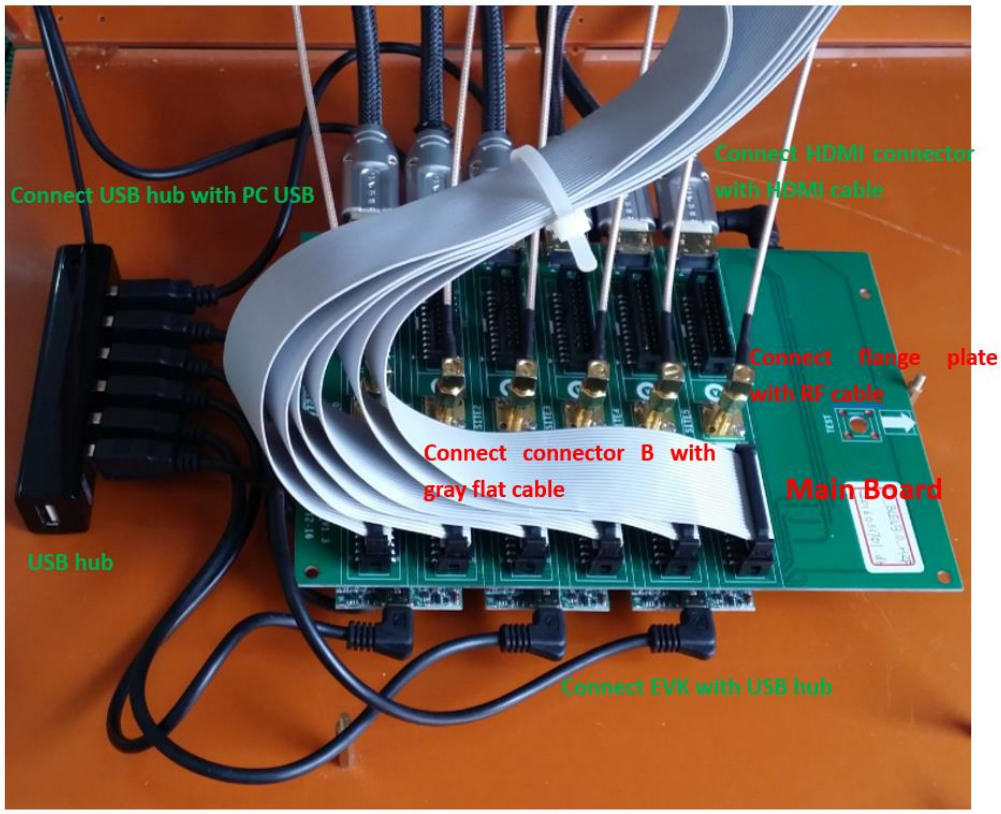

Figure 2-11 Cable connection sketch of main board

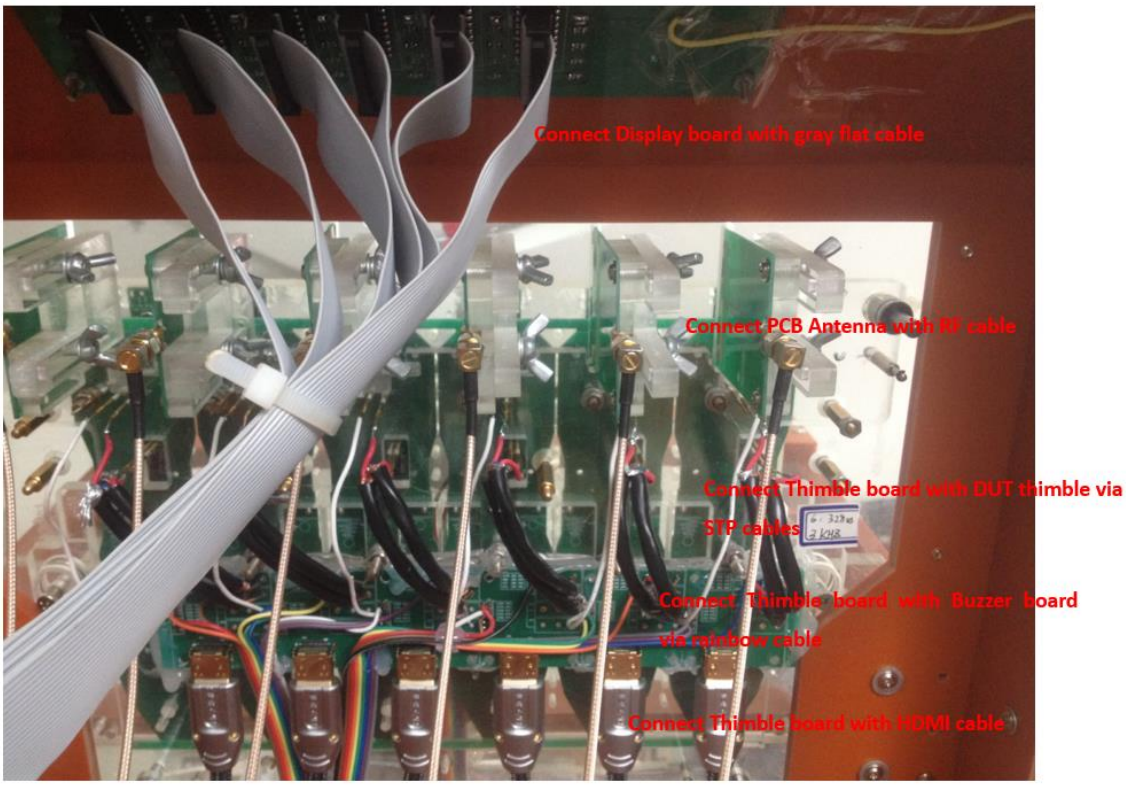

Figure 2-12 Cable connection of display, antenna, thimble board and DUT thimble

2.4 Check Jig Debugging

Keeping test consistency is critical for multiple sets of 1x6Jig. During debugging, it's needed to select several good products and several rejected products, then test them on each Site of each Jig; good products should pass test on each Site, and each rejected product should fail at the same test item on each Site. Take the rejected products with low RF Tx power for example, the data log is shown as follows:

Table 2-3 Test record of the failed product on the test jig

Site NO	Board NO	Channel	TX Test	Offset	RX Test	IEEE Address
1	star	2392	100/-34	2	-	-
		2495	-	9	-	
	1st ok	2392	100/-26	6	92/-54	0x8a003a30
		2495	100/-26	12	100/-54	

	2nd ok	2392	100/-29	-9	96/-62	0x8a003a36
		2495	100/-27	-4	100/-54	
2	star	2392	100/-29	1	-	-
		2495	100/-32	7	-	
	1st ok	2392	100/-23	4	100/-53	0x8a1019ec
		2495	100/-25	12	100/-54	
	2nd ok	2392	100/-23	1	100/-54	0x8a1019f2
		2495	100/-25	11	100/-53	
3	star	2392	100/-31	-7	-	-
		2495	100/-32	-1	-	
	1st ok	2392	100/-23	-2	100/-53	0x8a203d21
		2495	100/-25	4	100/-54	
	2nd ok	2392	100/-25	-17	100/-54	0x8a203d27
		2495	100/-25	-9	100/-54	
4	star	2392	100/-32	4	-	-
		2492	-	-	-	
	1st ok	2392	100/-25	7	99/-54	0x8a301f13
		2492	100/-25	11	100/-54	
	2nd ok	2392	100/-25	-8	100/-54	0x8a301f19

		2492	100/-26	-4	100/-54	
5	star	2392	100/-32	-3	-	-
		2495	-	-	-	
	1st ok	2392	100/-25	2	100/-54	0x8a401fcc
		2495	100/-25	8	100/-54	
	2nd ok	2392	100/-26	-14	88/-53	0x8a401fd3
		2495	100/-25	-6	100/-54	
6	star	2392	96/-33	-2	-	-
		2495	-	-	-	
	1st ok	2392	100/-28	2	100/-56	0x88403d0a
		2495	100/-26	7	100/-54	
	2nd ok	2392	100/-26	-13	100/-54	0x88403d11
		2495	100/-26	-6	100/-54	

If the rejected products with low RF Tx power output high power on some Site, or even pass test, by tuning height of external PCB antennas, RF energy can be effectively adjusted to keep consistency of test result. To weaken RF energy, increase the distance between external PCB antenna and PCBA; to strengthen RF energy, decrease the distance between external PCB antenna and PCBA.

3. Appendix

3.1 Appendix 1： Hardware List

Table 3-1 Hardware list

Type	Number	Spec	Note
Main board	1	C1T42A19_V1.4	Assembled on the main board
BLE EVK daughter board	6	C1T42A20_V3.3	
Power board	1	C1T42A36_V2.0	
Flange plate	6	MA-SMA-KKF 2-head flange	
Screw	12	PM2.5X8 screw	
Nut	12	M2.5 nut	
Short RF cable	6	SMA-MMCX cable 4cm	
HDMI cable	6	HDMI1.4A/A-A interface/50cm	-
Thimble board	6	C1T42A19_V3.1	-
Buzzer board	6	C1T64A3_V2.0	Not supplied by default. Only supplied for DUT with MIC.
STP (Shielded Twisted Pair) cable	1	2-cord/RV0.5/1.2m	-
External antenna board	6	ANT_01	-
Long RF cable	6	SMA90°-SMA90° cable-30cm	-

Display board	1	C1T42A19_V2.2	-
FC-40P gray flat cable	6	2-end 2.54mm*2*12/28AWG/ 105℃/Grey/50cm	-
18P rainbow cable	1	18-cord/16AWG/1m	-
Power adapter	1	Lenovo ADP-90DD B Input: 100-240V 1.5A Output: 20V 4.5A	-
USB2.0 hub	1	Unitek/7 interfaces/USB2.0 hub	-
Micro USB cable	6	USB2.0/28AWG/30cm, 90°/30V/80℃/A3-B	-
Carton, size 6	1	Standard 3-layer 260*150*180mm	-

3.2 Appendix 2： Pins on Test Site of Main Board

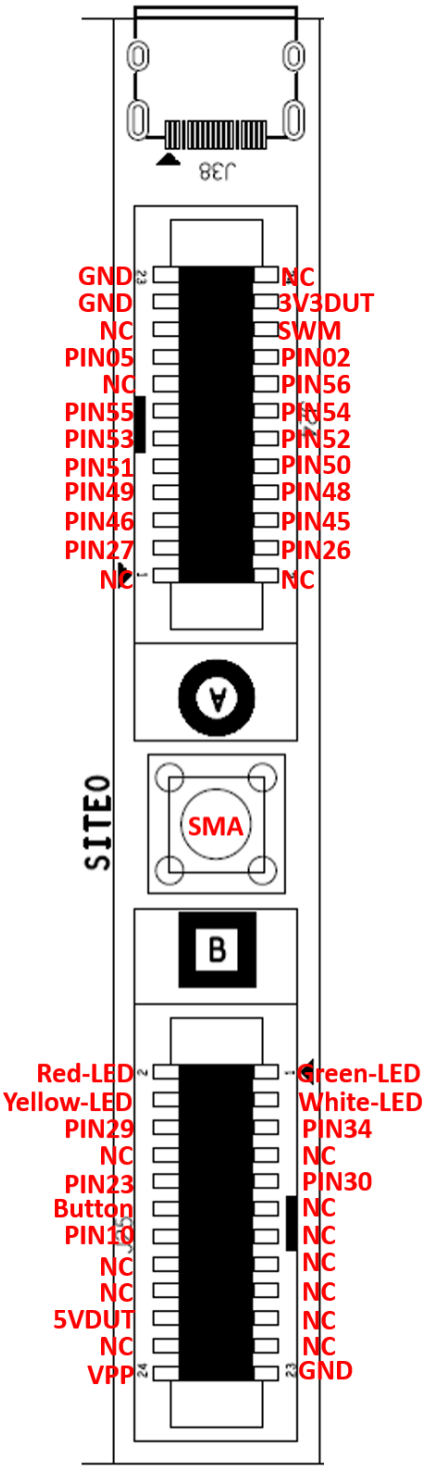

Figure 3-1 Pins on test site of main board

Note

- *In Figure 3-1, NC indicates no connection.*
- *Test pins on connector A should be connected by using STP (Shielded Twisted Pair) cables.*

3.3 Appendix 3: Dimension Chart of Main Board, Thimble Board, Display Board, EVK Daughter Board and Buzzer Board

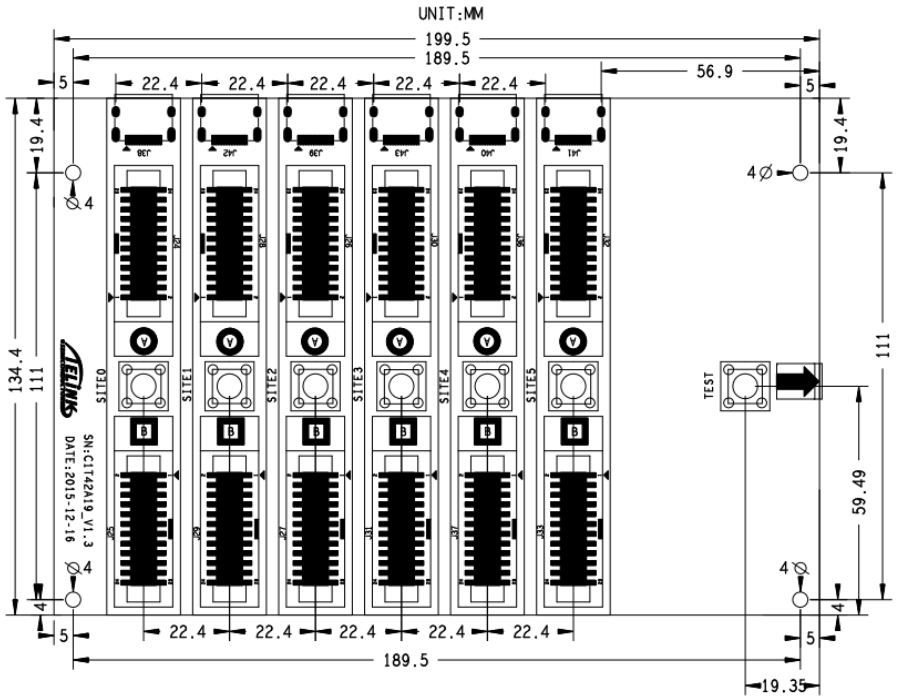

Figure 3-2 Dimension chart of main board

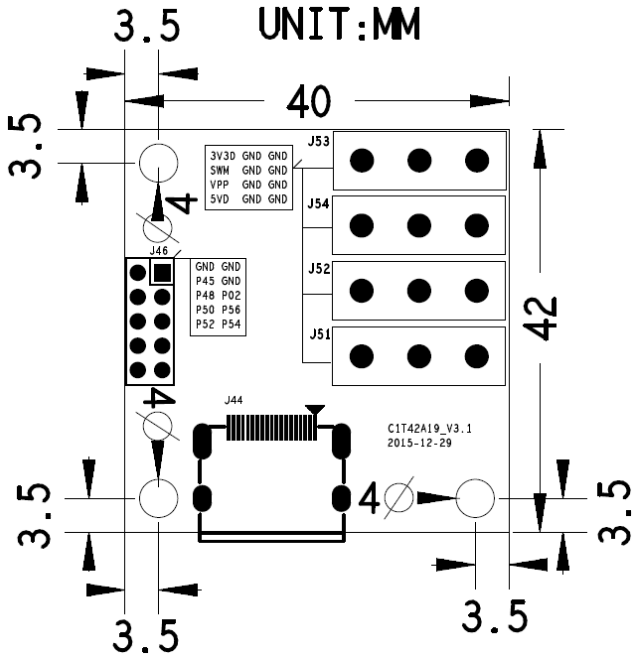

Figure 3-3 Dimension chart of thimble board

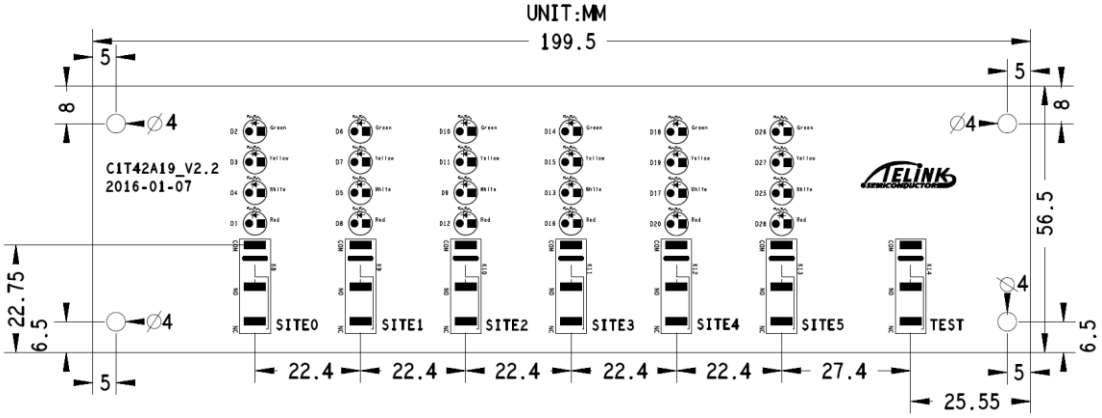

Figure 3-4 Dimension chart of display board

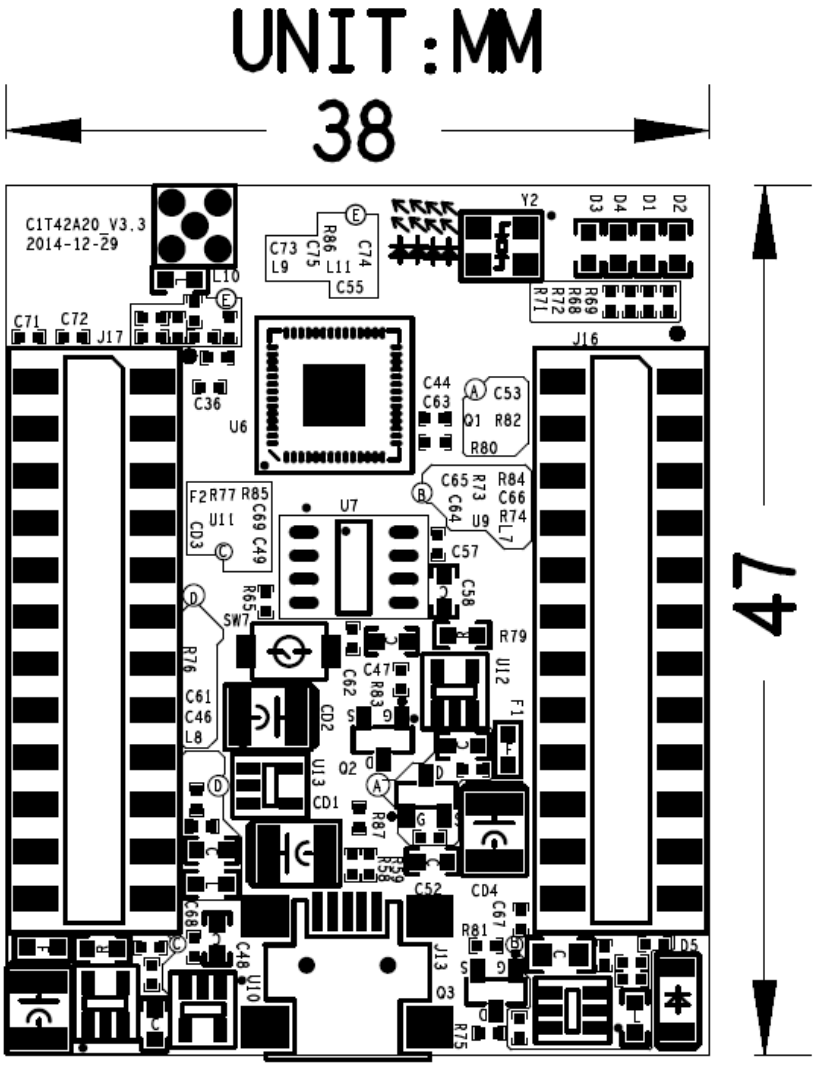

Figure 3-5 Dimension chart of EVK daughter board

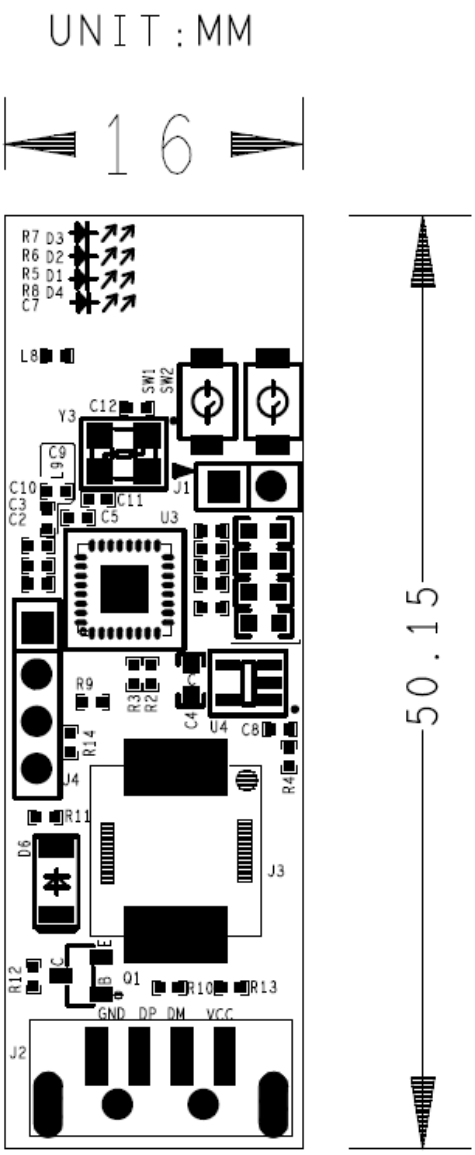

Figure 3-6 Dimension chart of buzzer board