Memo: TLSR951x Errata

From: Telink Semiconductor

Data: 2021/01/06

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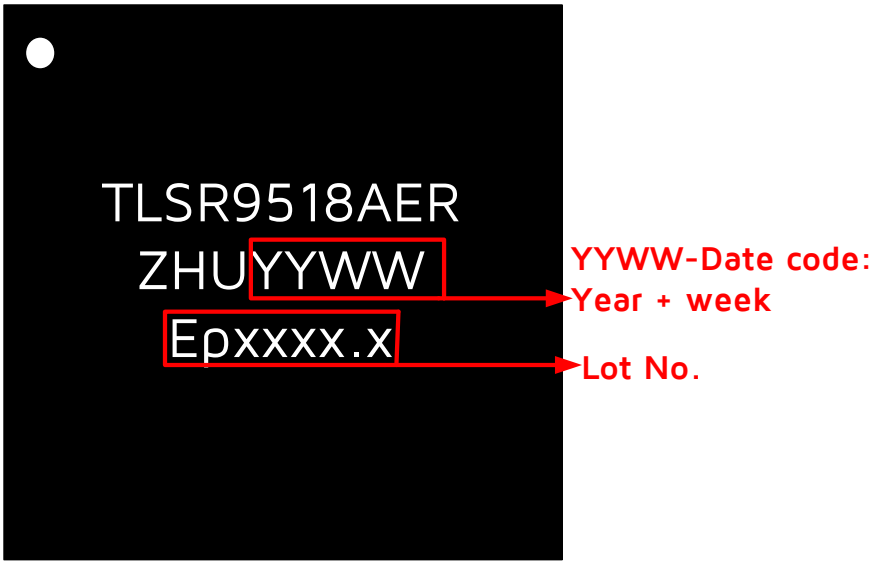
1. Introduction

This document presents Errata information for the TLSR951x chip A0 and A1 version engineering sample (ES). This document applies to the chip with marking shown below.

Product Series	Lot. No.	Version ID
TLSR951x A0 Version	EP8616& EP8616.69	0xFF
TLSR951x A1 Version	EP9044.12& EP9044.13	0xFE
TLSR951x A2 Version	EP9327.14	0xFA

Note: Version ID can be read from register 0x140e02[1:0].

The SoC is marked as following (take TLSR9518 as an example),


TLSR9518AER
ZHUYYWW
Epxxxx.x
YYWW-Date code:
Year + week
Lot No.

2. Change Log

Version	Major Changes	Date	Author
1.0.0	Initial release	2020/09	SY, SGJ
1.0.1	Update document format	2020/09	SY, YH
1.0.2	Update A1 related information	2020/10	SY, YH
1.0.3	Updated A2 related information	2021/01	SY, YH

3. Anomaly History

Item	Description	Chip Version		
		0x00(A0)	0x01(A1)	0x02(A2)
Power on failed	Chip cannot power on when Vbat is above 2.8V	-	New	Fixed
32KHz Crystal function failed	32KHz Crystal cannot work	-	New	Fixed
PD[0] function failed	PD[0] cannot work	-	New	Fixed
SDP Function Failed	Only JTAG and SWS could be used for debug function	-	New	New
Trickle mode in Charger	Charger cannot work in trickle charge mode	New	Fixed	-

Item	Description	Chip Version		
		0x00(A0)	0x01(A1)	0x02(A2)
Leakage in Deep Retention Mode	The power consumption in deep with retention mode is larger than the design target.	New	Fixed	-
Suspend Mode	The SoC cannot work under suspend low power mode.	New	Fixed	-
IO Glitch during Wake up	When the chip is waken up from the lower power mode, a glitch will be observed on some GPIOs	New	Fixed	-
GPIOs on PD0 ~ PD7	PD0~PD7 cannot be used in application.	New	Fixed	-
SAR ADC	SAR-ADC are not able to be used in application.	New	Fixed	-
USB Packet-Sending Issue	USB packet sending issue	New	Fixed	-

Please check Lot No. and Version ID for chip version.

4. Anomalies of Version 0x02(A2)

4.1 Overview

Item	Description	Reference
SDP Function Failed	Only JTAG and SWS can be used for debug function	4.2

4.2 SDP Function Failed

Issue symptom:

A1/A2 version is only able to be debug via JTAG and SWS interface. The SDP mode in PE[6]/PE[7] could not work. Other function in PE[6]/PE[7] could work.

Consequence:

SDP Function Failed

Workaround:

Only JTAG and SWS can be used for debug function

5. Anomalies of Version 0x01(A1)

5.1 Overview

Item	Description	Reference
Power on failed	Chip cannot power on when Vbat is above 2.8V	5.2
32KHz Crystal function failed	32KHz Crystal cannot work	5.3
PD[0] function failed	PD[0] cannot work	5.4

5.2 Power on failed

Issue symptom:

A1 version is only able to start with battery supply lower than 2.8V or directly supply from USB 5.0V. For battery voltage above 2.8V, it is not working. After power on with battery supply lower than 2.8V or directly supply from USB 5.0V, A1 version can work under battery supply between 1.8V to 4.2V.

Consequence:

Cannot power on with battery voltage above 2.8V.

Workaround:

Selecting one way as below,

1. Can power on and work directly supply from USB 5.0V(a battery need to be connected to VBAT);

2. Can work under battery supply lower than 2.8V;

3. Using external LDO or DCDC to generate the 2.8V supply from batter supply.

Fixed in the A2 version.

5.3 32KHz Crystal function failed

Issue symptom:

One analog control register is changed in A1 version, causing 32KHz crystal Oscillator not working.

Consequence:

32KHz crystal Oscillator cannot work.

Workaround:

Use 32KHz RC Oscillator as the low power timer.

Fixed in the A2 version.

5.4 PD[0] function fails

Issue symptom:

One analog control register is changed in A1 version causing the PD[0] not working.

Consequence:

PD[0] cannot work.

Workaround:

Trying to use other GPIO.

Fixed in the A2 version.

6. Anomalies of Version 0x00(A0)

6.1 Overview

Item	Description	Reference
Trickle mode in Charger	Charger cannot work in trickle charge mode	6.2
Leakage in Deep Retention Mode	The power consumption in deep with retention mode is larger than the design target.	6.3
Suspend Mode	The SoC cannot work under suspend low power mode.	6.4
IO Glitch during Wake up	When the chip is waken up from the lower power mode, a glitch will be observed on some GPIOs	6.5

Item	Description	Reference
GPIOs on PD0 ~ PD7	PD0~PD7 cannot be used in application.	6.6
SAR ADC	SAR-ADC are not able to be used in application.	6.7
USB Packet-Sending Issue	USB packet sending issue	6.8

6.2 Trickle mode in charger

Issue symptom:

Normally in the trickle charge mode, when the voltage on VBAT is lower than the Vfast threshold, the current drops to approximately 10% of the fast charge current. But, in A0 version, the Charger couldn't provide the trickle current in trickle charge mode

Consequence:

Charger cannot work under the trickle working mode in A0 version.

Workaround:

In A0 version, disable the internal charger, when battery voltage is lower than 3.0V, to avoid large charge current to battery.

Fixed in the A1 version.

6.3 Leakage in Deep Retention Mode

Issue symptom:

There is a P/N junction from retention LDO to digital power domain. That will cause P/N junction inverse leakage around 0.8uA and making the deep in retention mode current larger than expected.

Consequence:

The power consumption in deep with retention mode is around 0.8 ~ 1uA larger than the design target.

Workaround:

Fixed in the A1 version and the deep current value will be decreased next version.

6.4 Suspend mode

Issue symptom:

After entering the suspend mode around 20ms later, some GPIOs working status will be changed, like from input to output, pull up enabled, etc. Also, that will cause some bigger current in suspend mode.

Consequence:

Chips aren't able to work under suspend low power mode.

Workaround:

Fixed in the A1 version.

6.5 IO Glitch during Wake up

Issue symptom:

When the chip is waken up from the lower power mode, a glitch will be observed on some GPIOs (PA0, PA2, PA4, PA5, PA6, PB2, PB4, PB5, PB6, PB7 and PE0), the width of glitch is less than 10us.

Consequence:

That glitch on GPIO might affect the external components or circuit.

Workaround:

In A0 version, regarding the total solution on system level, try to avoid connecting the circuit to PA0~PA7, PB0~PB7, which will be affected by the glitch during wake up process.

Fixed in the A1 version.

6.6 GPIOs on PD0~PD7

Issue symptom:

PD0~PD7 are not able to work for any function.

Consequence:

PD0~PD7 cannot be used in application.

Workaround:

Fixed in the A1 version.

6.7 SAR ADC

Issue symptom:

SAR-ADC are not able to work for any function.

Consequence:

SAR-ADC are not able to be used in application.

Workaround:

In A0 version, the low power comparator could be used for some basic analog signal recognition application, like battery voltage detection.

Fixed in the A1 version.

6.8 USB Packet-Sending Issue

Issue symptom:

Endpoint 0 can't send out a zero-length packet to indicate the completion of IN transfer, if the length of total IN payload is exactly an integer multiple of 8 bytes.

Consequence:

The USB device cannot send out an empty packet, it will send out a stall packet. This will cause problem during the enumeration process or vendor command read operations.

Workaround:

1. USB descriptor: Avoid returning IN token with the total payload length of an integer multiple of 8byte (currently, it is mainly string descriptor)
2. Vendor command: When designing a vendor command, the USB device should avoid returning IN token with the total payload length of an integer multiple of 8byte.

Fixed in the A1 version.