Telink

Telink Semiconductor

B91 Hardware Design Guideline

2020-12

Scope

- Chip`s datasheet is the basic reference file of hardware design. This document will go through datasheet with hardware engineer and supplement some details. It will speed up projects after reading the document.
- Considering that the chip`s datasheet will be continuously updated, if there is any difference between this document and the chip`s datasheet, please refer to the latest version of the chip specifications.
- The version and link of the chip`s datasheet mentioned in this document are as follows:
  - http://wiki.telink-semi.cn/wiki/chip-series/TLSR9-Series/
- TLSR9518A is taken as an example to describe. And the content mentioned in the file applies to the TLSR9 chipset serials.

Schematic Design Guideline

Reference Schematic

- Reference Schematic:
  - Refer to chapter 3 (reference design).
  - TLSR9518D`s reference design are listed here.
    - Schematic and BOM are listed together.
  - The schematic is the design of minimum core system
    - Easy to copy into other designs.
    - Easy to count the cost at the stage of design-in.

Pin layout - 1

- Pin layout:
  - Refer to chapter 1.5 and 1.6, which is useful to create schematic and PCB footprint symbol.
  - Power pins:
    - Refer to chapter 4.6.3 and 4.6.4.
    - PIN15(VDD25_EF), only connected out on TLSR9518A. It is used by E-fuse. A decoupling capacitor, 1uF, is needed.
    - PIN21(VCAP), refer to the description on DS. A decoupling capacitor, 1uF, is needed.
    - PIN23(VREFP_CODEC), refer to the description on DS. A decoupling capacitor, 1uF, is needed.
    - PIN24(AVD)/PIN50(FVDD1V8)/PIN51(VDD1V8_O)
      - DCDC mode: a inductor is added on the path of PIN51, then connect it with PIN24/50 together.
      - LDO mode: PIN51 is floating, PIN24/51 are connected together.
    - PIN34/35, refer to the description on DS. A decoupling capacitor, 1uF, is needed.
    - PIN41(VBUS) , a decoupling capacitor, 1uF, is needed when charging Lion-battery. Otherwise, it can be floating.
    - PIN42(VBAT), power supply of chip. A decoupling capacitor, 1uF, is needed.
    - PIN43(VDD3_DCDC)/PIN52(AVDD3), connected together, a decoupling capacitor, 1uF, is needed.
    - PIN44(VDD1V4_O)/45(DVDD1V4)/46(AVDD1V4)/64(VLINE_PAD)
      - DCDC mode: a inductor is added on the path of PIN44, then connect it with PIN45/46/64 together
      - LDO mode: PIN44 is floating, PIN45/46/64 are connected together.

Pin layout - 2

- Pin layout:
  - RF pins:
    - PIN63(ANT) is RF port.
  - Crystal pins:
    - PIN65(XC1), PIN66(XC2) connect 24Mhz crystal.
  - Debug and download pin:
    - PIN3(SWS) should be connected to a test point which is used to download firmware.
    - PIN71/72/73/74 is a group of JTAG interface. Please refer to table 1-6 for detail.
    - A group UART pin should be connected to test points which is used to do BQB test.
      - Some BQB binary files have been prepared on WIKI.

Certification

- A Π type filter is used for matching to pass certification, the values of which are flexibly adjustable corresponding to layout.
- Firstly, use VNA (Vector Network Analyzer) to do RX matching.
  - Customers must power on DUT, and use EMI tool to configure chip into RX mode, then tune RX matching.
- After RX test is finished, SA (Spectrum Analyzer) should be used to check TX harmonic.
  - If harmonics do not meet the requirements, re-do RX matching.
    - Use the VNA to adjust component value to meet the impedance matching requirements, and then check TX harmonic again.
- It is recommend to mount a shielding box on PCBA for certification if customer can afford the cost. It is easy to pass certification and save time.
- TLSR9518A development board has passed FCC certification,
  - FCCID: OEOTLSR9518ADK80D

Crystal

- 24M Crystal:
  - Refer to table 2-8.
  - The recommended specifications are as follows:
    - 24Mhz – 12pF - +/-20ppm
  - The range of internal load capacitor is among 5pF~18pF.
- 32.768K crystal:
  - Refer to table 2-9.
  - PD0 and PD1 can be used to connect external 32.768Khz crystal.

Interface

- GPIO:
  - Refer to chapter 9.1.
    - All GPIO pins have configurable pull-up resistor and pull-down resistor.
    - All GPIO pins can be independently configured as high-level/low-level wakeup source.
- PWM:
  - Refer to chapter 10.
    - Up to 6 PWM output channels. Each PWMxn (x=0~5) has its corresponding inverted output pins, PWMxn_N pin.
    - PWM0 pins, including PWM0 and PWM0N, can be used as IR driver pin.

Interface(Cont.1)

- AMIC:
  - Refer to table 1-4.
  - Both differential mode and single mode are supported. Differential mode is preferred if differential mode is supported by the package.
- DMIC:
  - Refer to table 1-4.
  - Two groups of PINs can be configured as DMIC signal.
    - PB2/3/4 and PC1/2/3
- I2S:
  - Refer to table 1-4.
  - Supports one group I2S pins, PC3(bit clk)/PC4(output frame clk)/PC5(output data)/PC6(input frame clk)/PC7(input data).

Interface(Cont.2)

- UART:
  - Refer to table 1-4 and chapter 9.9.
  - Supports general UART interface and 7816 UART interface.
  - Any TX and RX can be configured into a group to use.
  - Two groups of UART are supported, UART0 and UART1.
    - PA1/2/3/4, PB2/3/4/6, PD0/1/2/3 can be configured as UART0.
    - PC4/5/6/7, PE0/1/2/3 can be configured as UART1.

Interface(Cont.3)

- I2C:
  - Refer to table 1-4 and chapter 9.3.
  - PB2/3, PC1/2, PE0/2 and PE1/3 can be configured as I2C.
  - For supporting up to 400K bit/s, external pull-up resistors must be added.
- SPI:
  - Refer to table 1-4, chapter 9.5/6/7/8.
  - Supports memory SPI, HSPI, PSPI and SPI_SLV.
  - PA1/2/3/4, which are slave mode in default mode, can be configured as HSPI with PB0/1.
  - HSPI supports master/slave mode, used in high performance application.
  - PSPI supports master/slave mode, used in low power application.

Interface(Cont4)

- ADC:
  - Refer to table 1-4 and chapter 12.
  - Supports up to 10 detect pins, including PB0~PB7, PD0~PD1.
- Battery voltage detect:
  - If the system is powered by two AAA batteries, the system can directly detect the voltage of VBAT.
  - When the system is powered by the lithium battery, it can be connected to the VBAT pin. A hardware voltage divider circuit should be used.
  - If the system is powered by only one AAA batteries, it needs to be connected to a boosted DCDC. Then, the battery voltage needs to be connected to an ADC pin for voltage detection. A voltage divider circuit needs to be added outside to make the voltage lower than 1.2V.

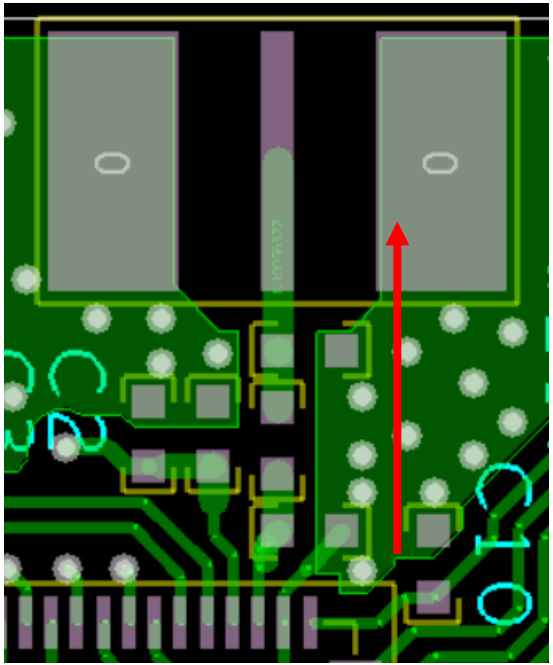
Interface(Cont.5)

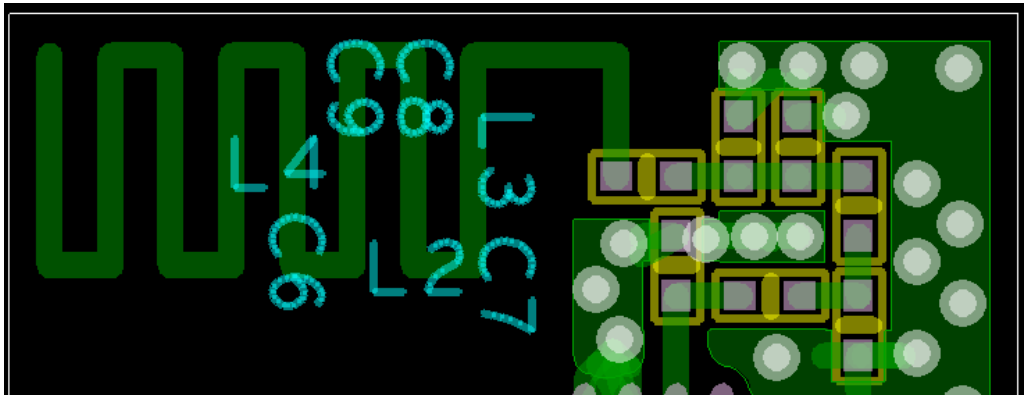
- External RF front-end pins:
  - Refer to table 1-4.
  - TXCYC is used to control the PA (Power Amplifier) of external RF Front-end: PB0, PD7, PE5.
  - RXCYC is used to control the LNA of external RF Front-end: PB1, PD6, PE4.
- Antenna Select pins:
  - Refer to table 1-4.
  - One groups of SEL<0:2>: PC0/PC1/PC2 are used to select one of up to eight external antennas. The selected antenna channel is connected to the RF_IO pin.

PCB Design Guideline

RF layout

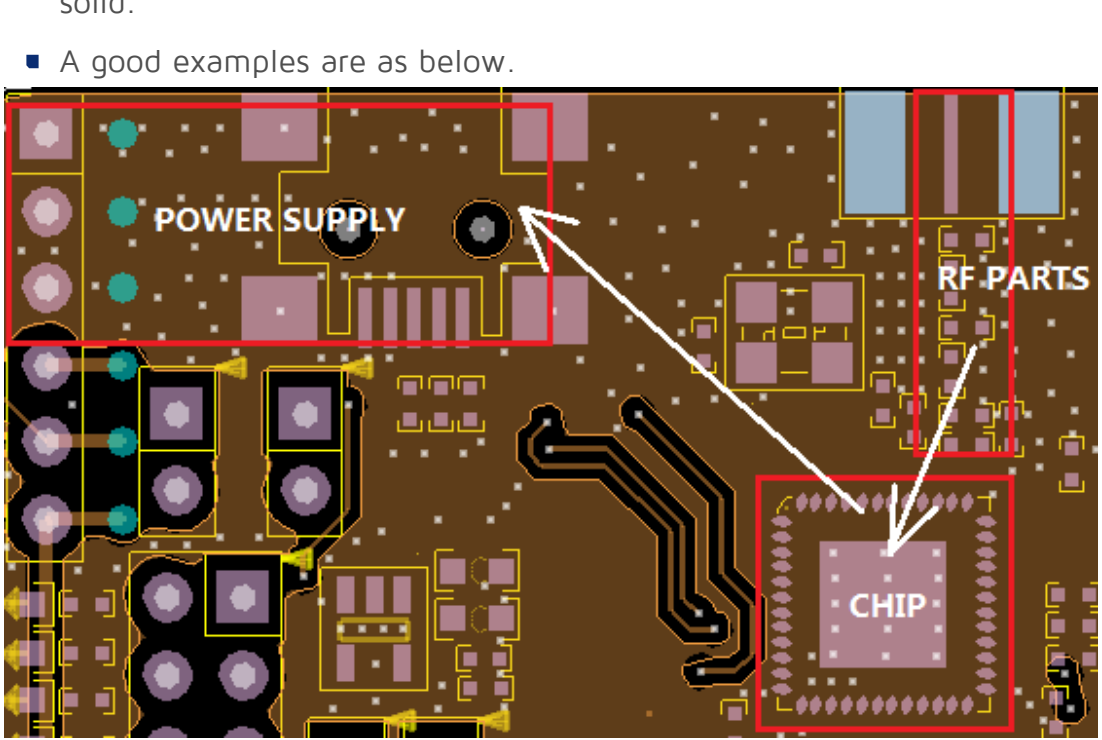
- The components on the RF path MUST be placed one by one. and they MUST be placed close to each other, no stub.
- It the area is not enough, can fold it, but MUST use ground and via to shield RF trace.

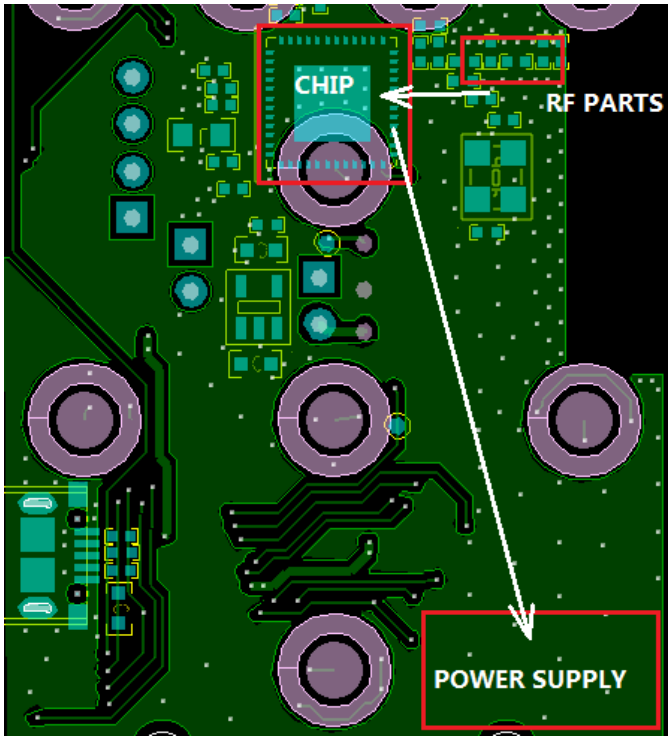




Solid Ground Plane

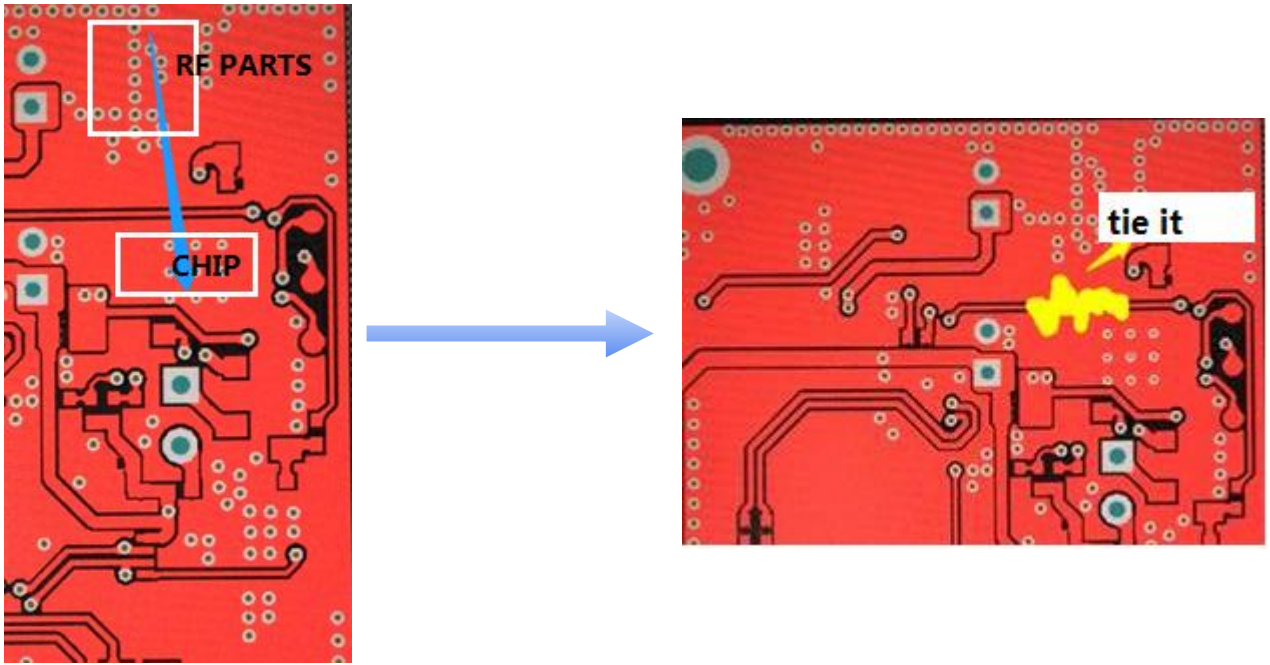
- The ground plane MUST be wide, solid. The ground plane from power supply to chip, then at last to RF parts MUST be solid.
- A good examples are as below.





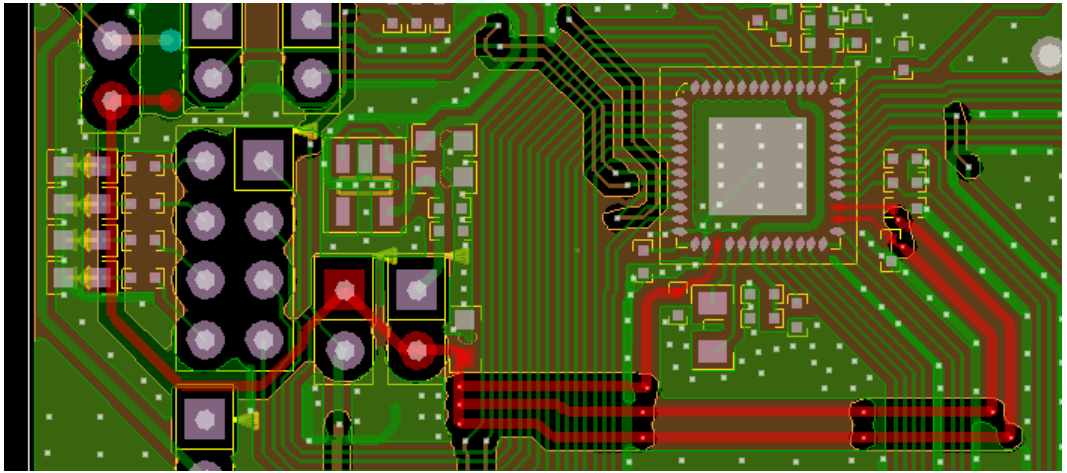
Solid Ground Plane(Cont)

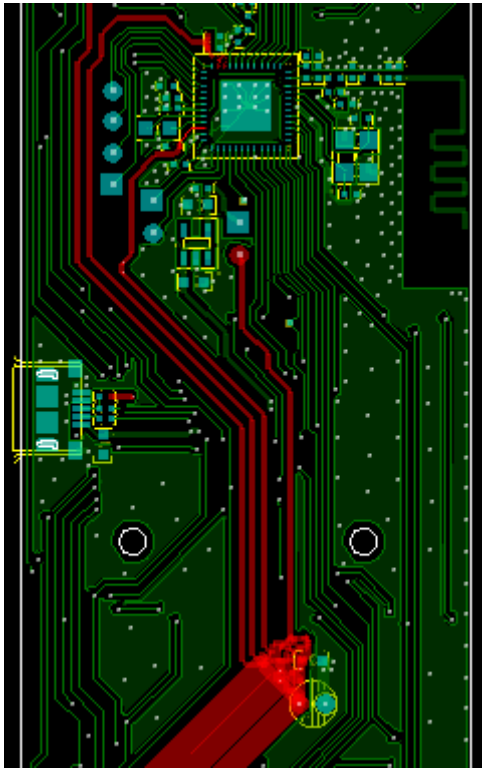
- A bad example is as below.
  - Ground plane between RF parts and chip is cut off, the rx performance is greatly affected.
  - Tie them together, the RX performance matches the data on the datasheet.



Star connection

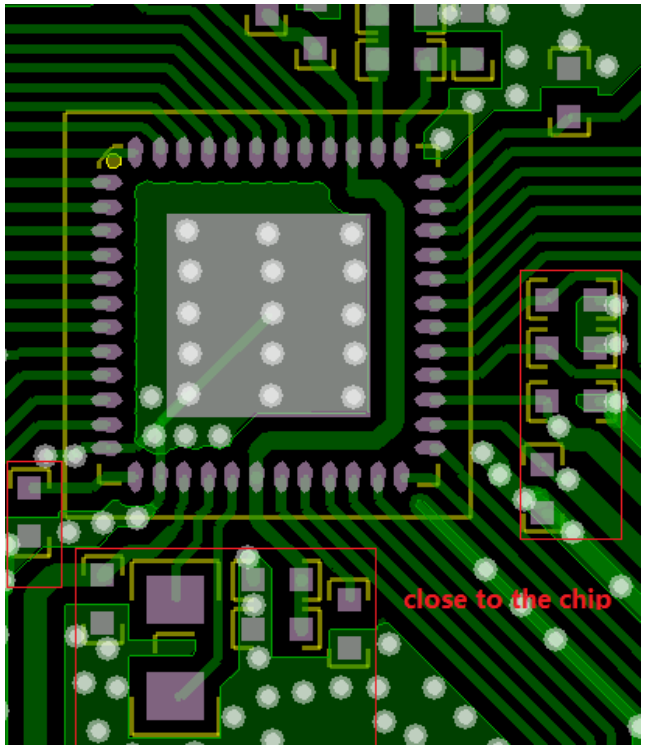
- Power supply should be connected in star-type connection.
  - If there is no audio function, can connect them together.

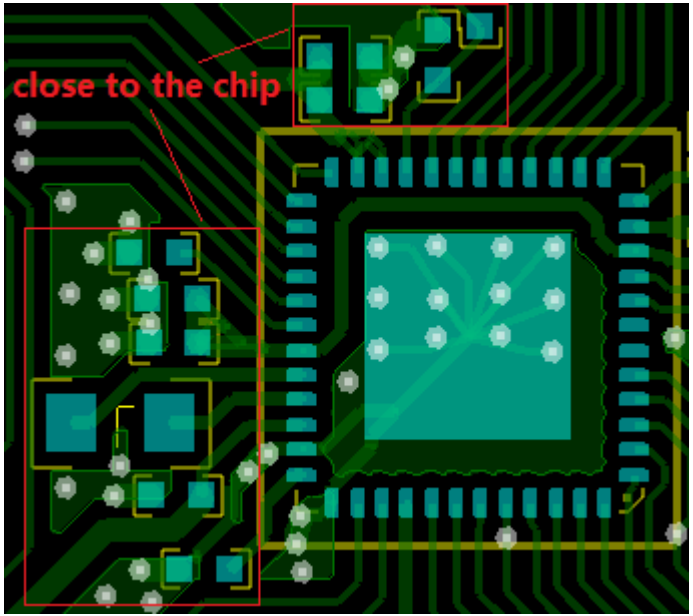




Decoupling capacitor

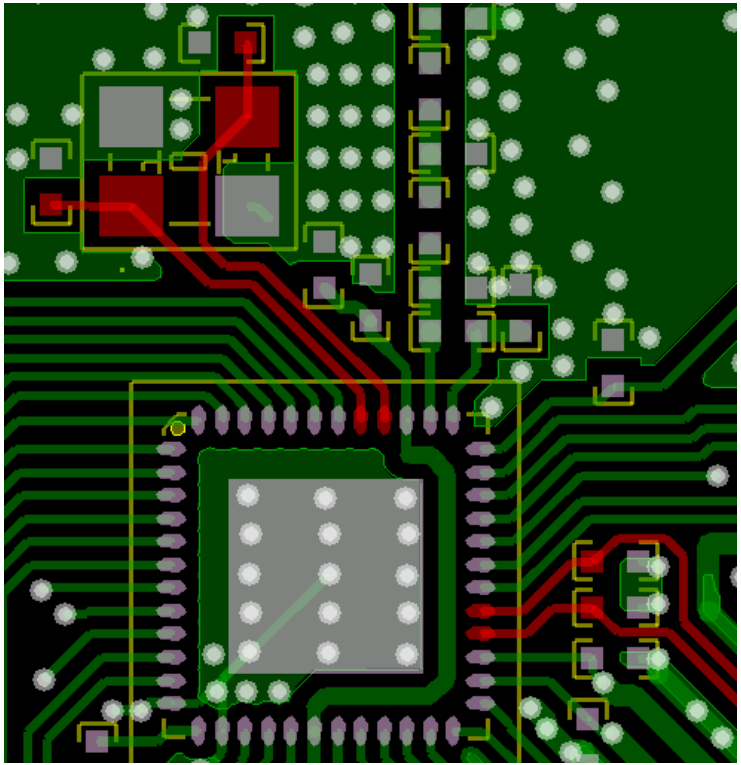
- Decoupling capacitors MUST be placed close to power pins.

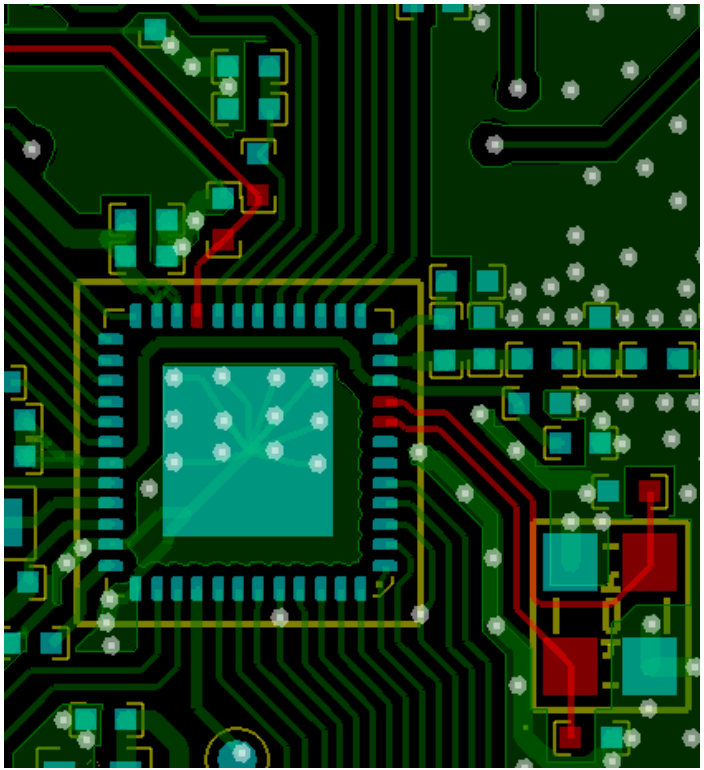




Key traces

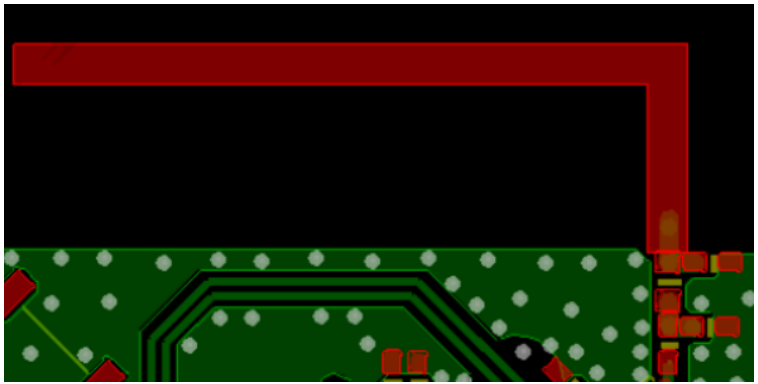
- To avoid EMI issue, some important parts such as crystal, audio trace, mic trace and usb trace MUST be shielded by GND and via.





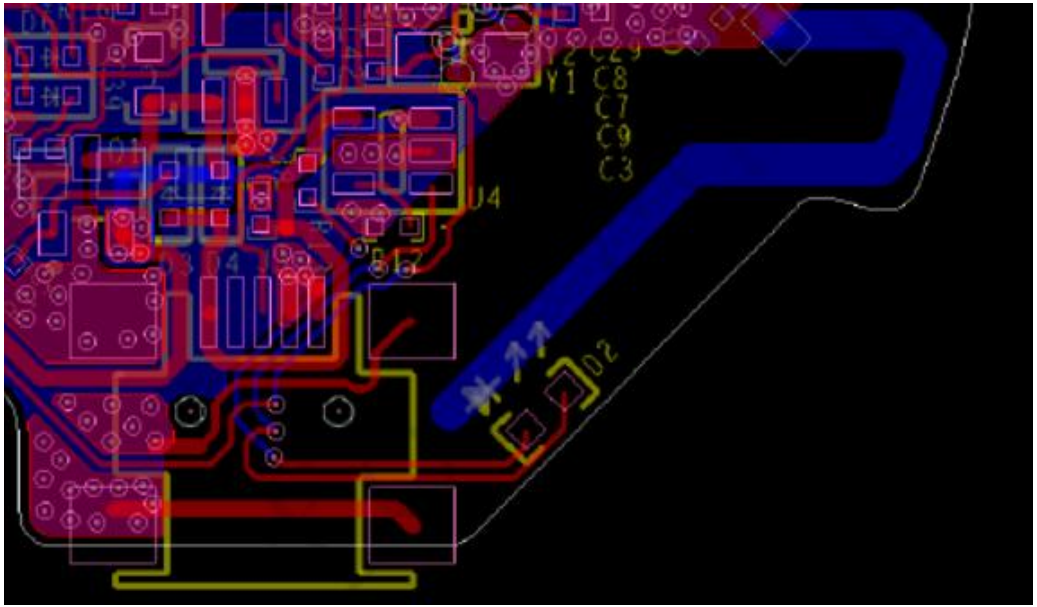
Antenna – common requirement

- Antenna trace width shouldn`t be too narrow in order to decrease loss.
- Line width should be 0.5mm or above, generally it`s recommended to be 0.5mm or 1mm.
- Top and bottom of antenna location should not be covered by GND.
- The distance between antenna and GND should be 3mm or above.
- Generally antenna length is 20mm~30mm. The smaller the GND is, the longer the antenna should be.



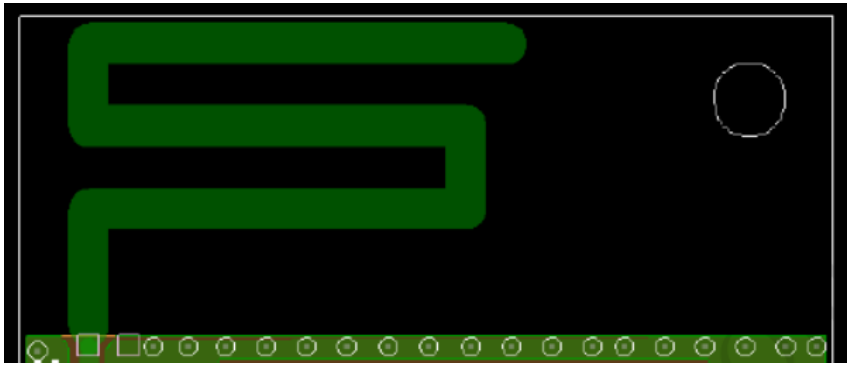
Antenna – keep away others

- Keep PCB antenna far away from metal, battery, or other components, such as 3mm or 5mm.
- A bad example is showed as below. The antenna is too close to USB connector.



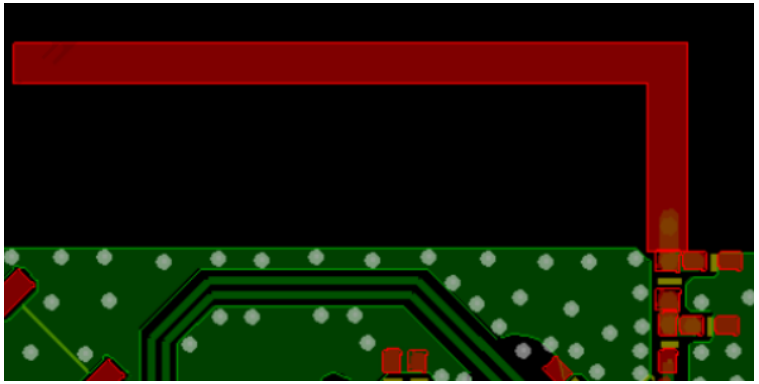
Antenna – don`t exposed to others

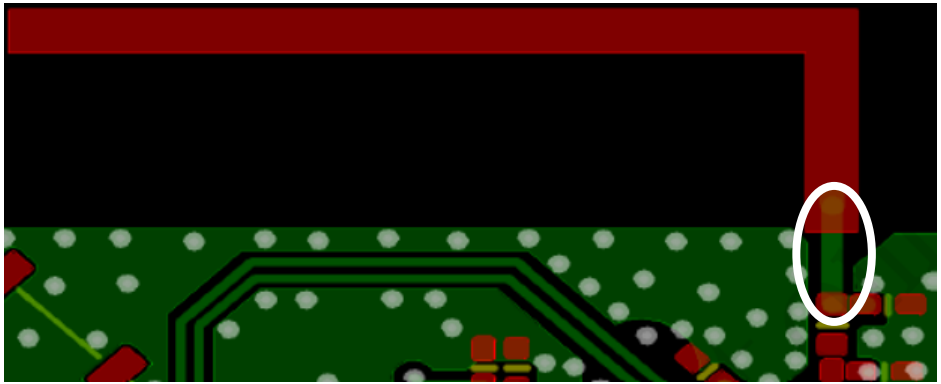
- There MUST be a row of via holes along the antenna on the side parallel to GND. Do not directly expose trace or pad to the antenna.
- The left is a good example. The right is a bad example.



Antenna – matching components

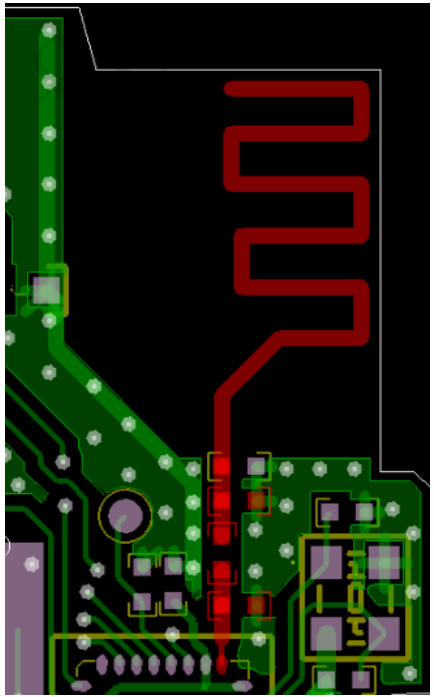
- Antenna matching components should be placed at the boundary of antenna and GND without shrink inward or expand outward.
- The left is a good example. The right is a bad example.

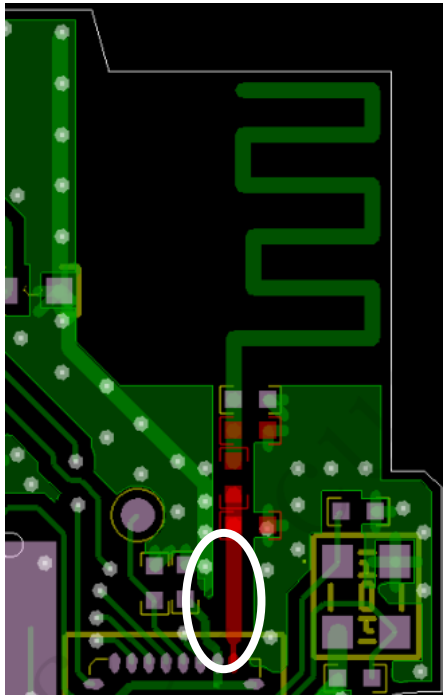




Antenna – impedance design

- The RF line to the antenna port should be short. If RF trace can`t be designed shortly, it must be designed as 50ohm micro-strip line.
- The left is a good example. The right is a bad example.





Change Logs

- 2021.01.05
  - Initial version