Telink

Telink Semiconductor

B92 Hardware Design Guideline

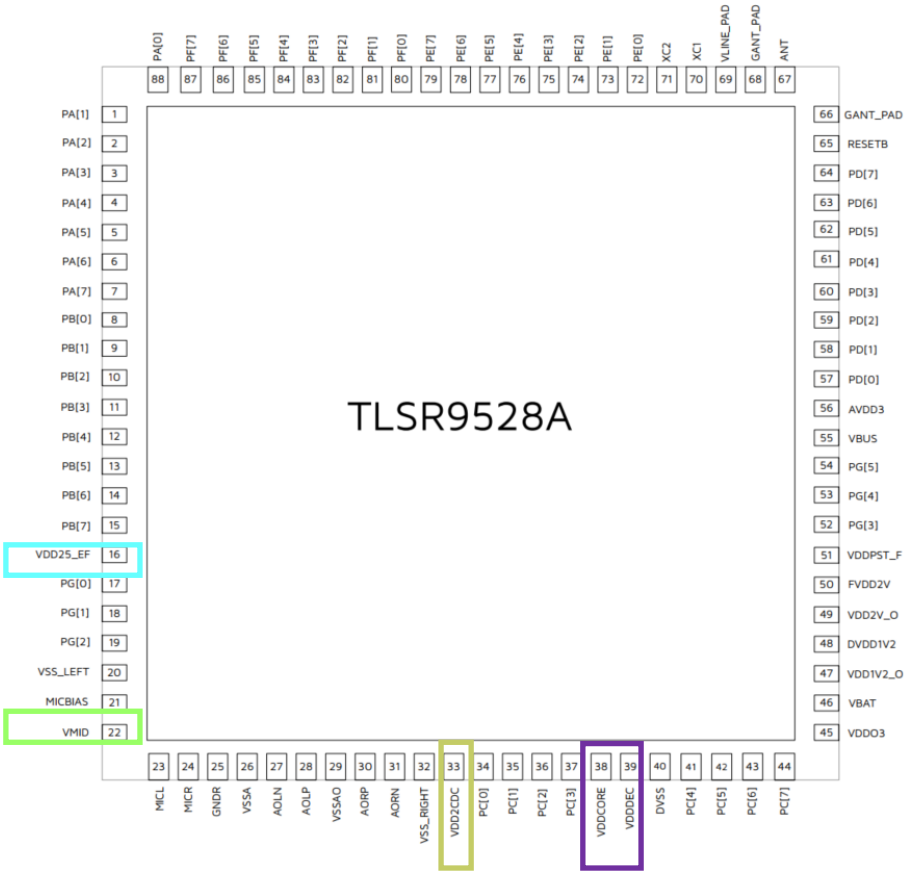
2023-3

Scope

- Chip`s datasheet is the basic reference file of hardware design. This document will go through the datasheet with the hardware engineer and supplement some details. It will speed up projects after reading the document.
- Considering that the chip`s datasheet will be continuously updated, if there is any difference between this document and the chip`s datasheet, please refer to the latest version of the chip specifications.
- The version and link of the chip`s datasheet mentioned in this document are as follows:
  - TBD
    - http://wiki.telink-semi.cn/wiki/chip-series/TLSR9-Series/
- TLSR9528A is taken as an example to describe. And the content mentioned in the file applies to the B92 chipset serials.

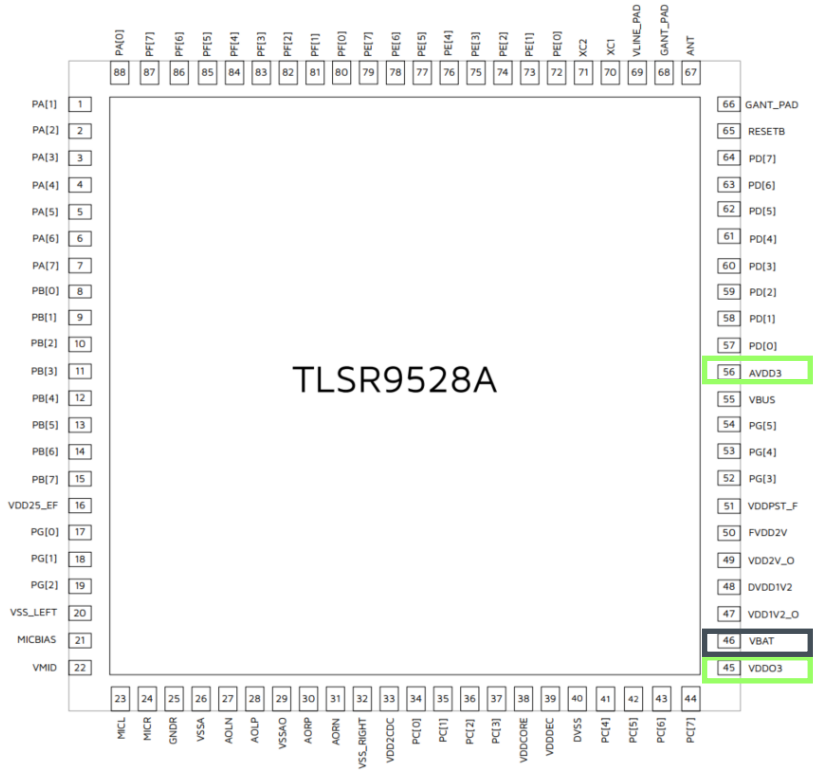
Schematic Design Guideline

Pin layout – Power Supplies : Part A



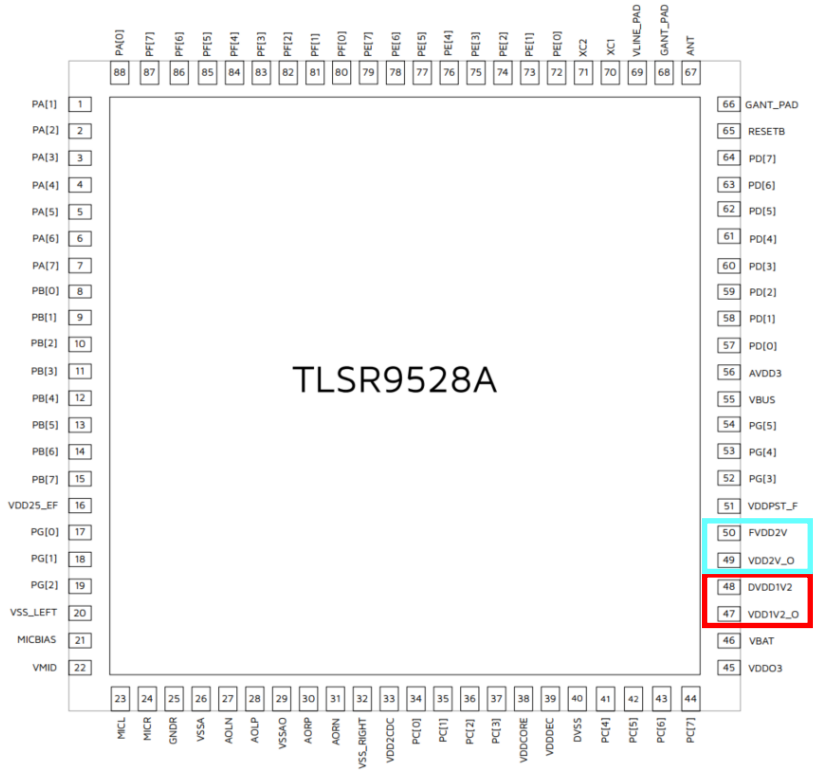
- PIN16(VDD25_EF):
  - E-fuse power supply pin.
  - A 1uF decoupling capacitor is required.
- PIN22(VMID):
  - Power pin of the embedded audio codec module.
  - A 1uF decoupling capacitor is required.
- PIN33(VDD2CDC):
  - Audio codec power supply pin. Usually connected to a 2V power source.
  - A 1uF decoupling capacitor is required.
- PIN38(VDDCORE)/PIN39(VDDDEC):
  - These two pins should be connected. And a 4.7uF decoupling capacitor is required.

Pin layout – Power Supplies : Part B



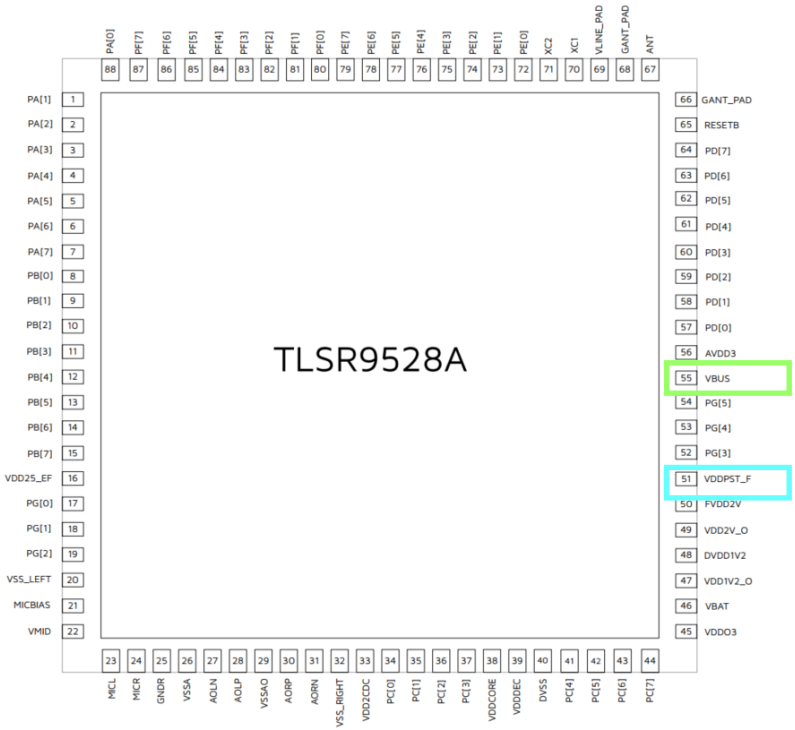
- PIN45(VDDO3)/PIN56(AVDD3):
  - These two pins should be connected. A 1uF decoupling capacitor is required.
  - Power supply for all GPIOs. PIN45 is the source, and PIN56 is the sink.
  - For some PN, vddo3 can be trimmed to 1V8.
- PIN46(VBAT):
  - Battery positive terminal. The power range is 1.8V~4.3V.
  - A 10uF decoupling capacitor is required.
  - If USB VBUS(5V) is available in the application, a external LDO or DCDC is recommended to use for converting 5V to 1.8V~4.3V for the VBAT pin.

Pin layout – Power Supplies : Part B



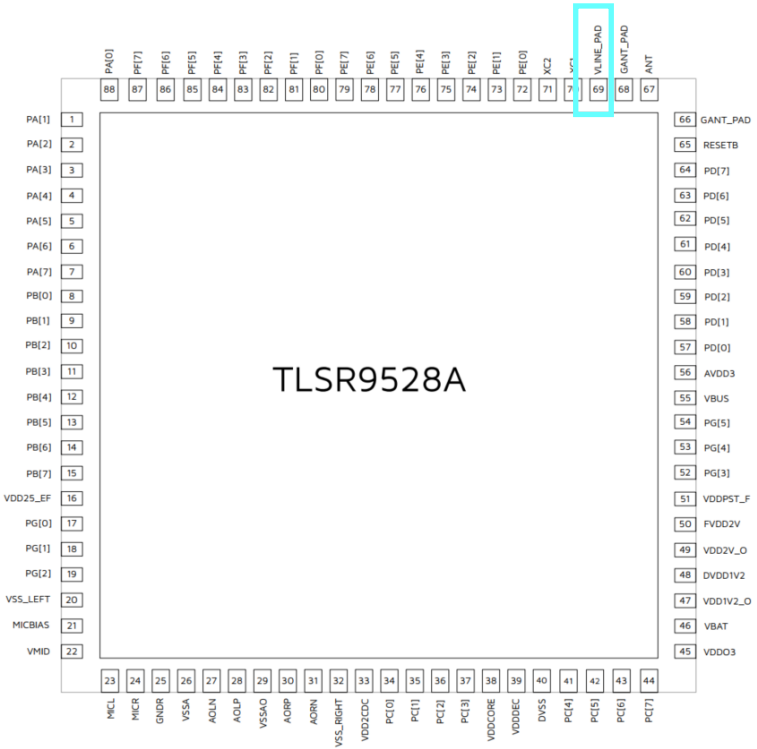
- PIN47(VDD1V2_O)/PIN48(DVDD1V2):
  - PIN47 is 1p35V DCDC Source, while PIN48 is the LDO Source.
  - PIN69 is 1p35V Sink.
  - In the application, DCDC mode is suggested for reducing consumption.
  - Some decoupling capacitors are required(see reference design).
- PIN49(VDD2V_O)/PIN50(FVDD2V):
  - PIN49 is 2V0 DCDC Source, while PIN50 is 2V0 LDO Source.
  - PIN33 is 2V0 Sink.
  - In the application, LDO mode is suggested considering the stable operation of flash.
  - Some decoupling capacitors are required(see reference design).

Pin layout – Power Supplies : Part C



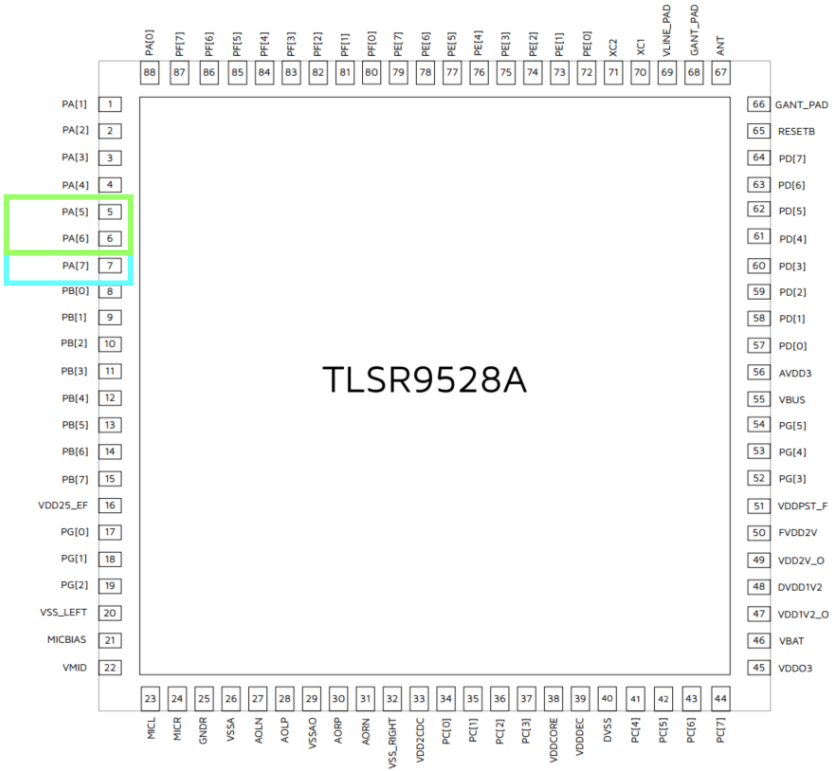
- PIN51(VDDPST_F):
  - Flash power supply generated by embedded 1V8 LDO.
  - A 1uF decoupling capacitor is required.
- PIN55(VBUS)
  - VBUS is the power supply for SOC, the voltage range is 4.5 V ~ 5.5 V. A 1uF decoupling capacitor is required.
  - When using VBUS instead of VBAT supply for TLSR9528A, hardware design should connect VDDO3 with VBAT.
    - When not powered by VBUS, don`t connect it to anything.
  - When 4.5 V ~ 5.5 V is applied at VBUS, the SOC can generate a reset signal after around 8 seconds.

Pin layout – Power Supplies : Part D



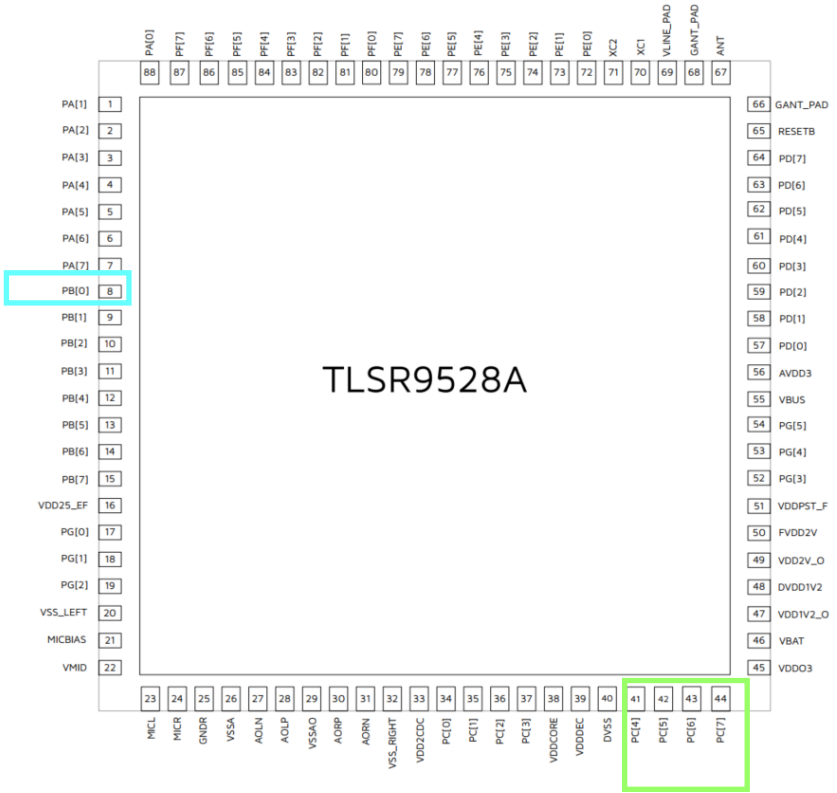
- PIN69(VLINE_PAD):
  - RF power supply pin.
  - 2.2uF&0.1uF decoupling capacitors are required.

Pin layout – Debug Port : Part A



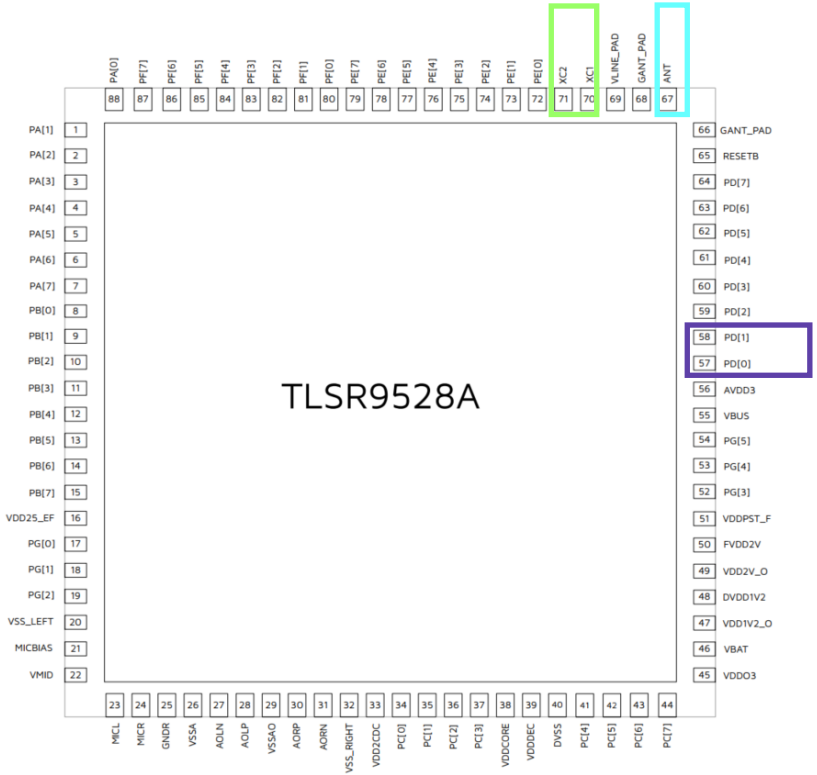
- PIN7(PA7/SWS):
  - Debug/Download pin
  - In the application, it must be connected to a test point.
  - A matching resistor in series is required
- PIN5(PA5_DM)/PIN6(PA6_DP):
  - USB interface.
  - Recommend connecting to test points for capturing logs when FW works.
  - Can’t works when vddo3 is set as 1V8

Pin layout – Debug Port : Part B



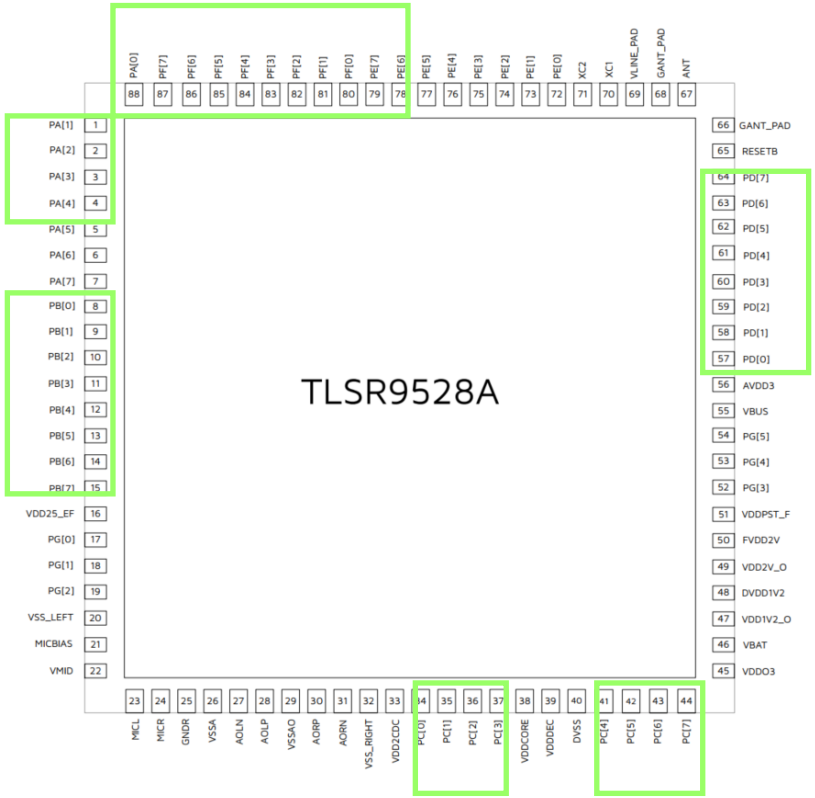
- PIN41/PIN42/PIN43/PIN44:
  - A group of JTAG interface, supports 2-wire(SDP) or 4-wire(JDP) mode.
  - When using SDP, the pins of PC [6] and PC [7] should be used. At this time, PC [4] and PC [5] can be used for other functions.
  - PB[0] is for choosing between SDP & JDP:
    - PB[0] pull-up: SDP
    - PB[0] pull-down: JDP
  - When power on or after coming back from deep sleep mode, SoC will read the PB[0] level, then the debug port is decided. Can not be modified through the init process or register.

Pin layout – RF Part: Part A



- RF Port:
  - PIN67(ANT) is RF port.
  - A 4th-order LC filter is recommended to use for certification. The details will be introduced in the next page.
  - In the application, we suggest remaining a TVS diode to prevent ESD risk.
- 24Mhz Crystal:
  - PIN70(XC1), PIN71(XC2) connect 24Mhz crystal.
  - Usually recommended specification: 24Mhz – 12pF - +/-10ppm
    - Sometimes try different kinds of 24Mhz crystal with different load capacitors, such as 10pf, and 15pf because of different PCB layouts to get lower frequency offset.
    - For some BLE projects, it is recommended to use the same type of crystal for both master and slave roles and to verify and calibrate the frequency bias according to different PCBs.
  - SOC has internal capacitors designed for the crystal. The range of the internal capacitor is 5pF~18pF.
- 32.768K crystal:
  - PD0 and PD1 can be used to connect external 32.768Khz crystal.

Pin layout – RF Part: Part B

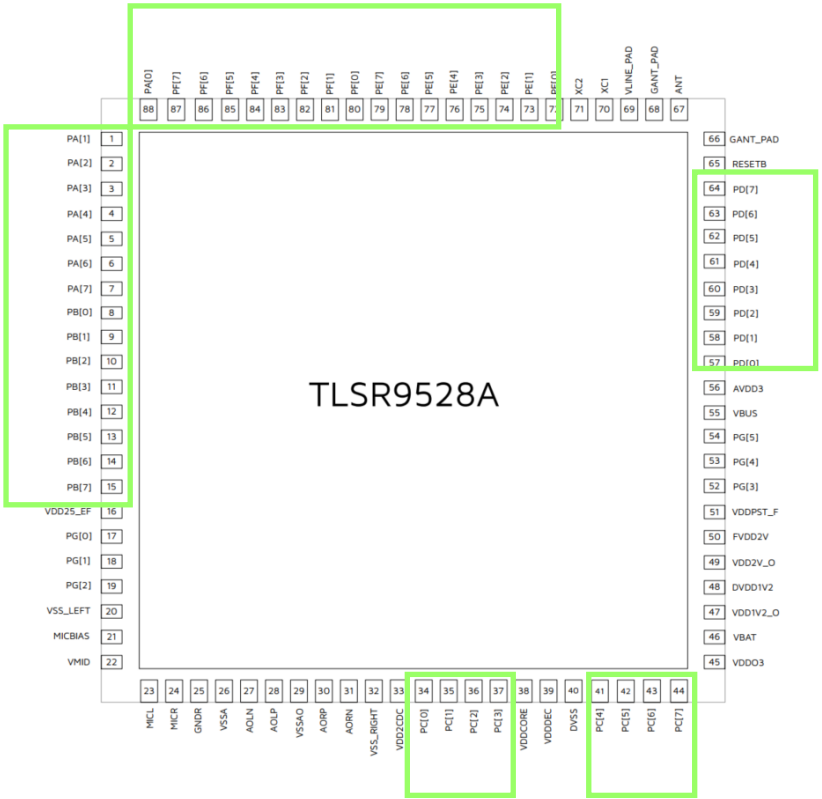


- External FEM(front end module) Control Port:
  - All GPIOs in the green box can be combined arbitrarily and configured as RX_ CYC2LNA or TX_ CYC2PA
  - TX_ CYC2PA connects TX of external FEM_ EN, RX_ CYC2LNA connects RX of external FEM_ EN

Pin layout – RF Part: Part C

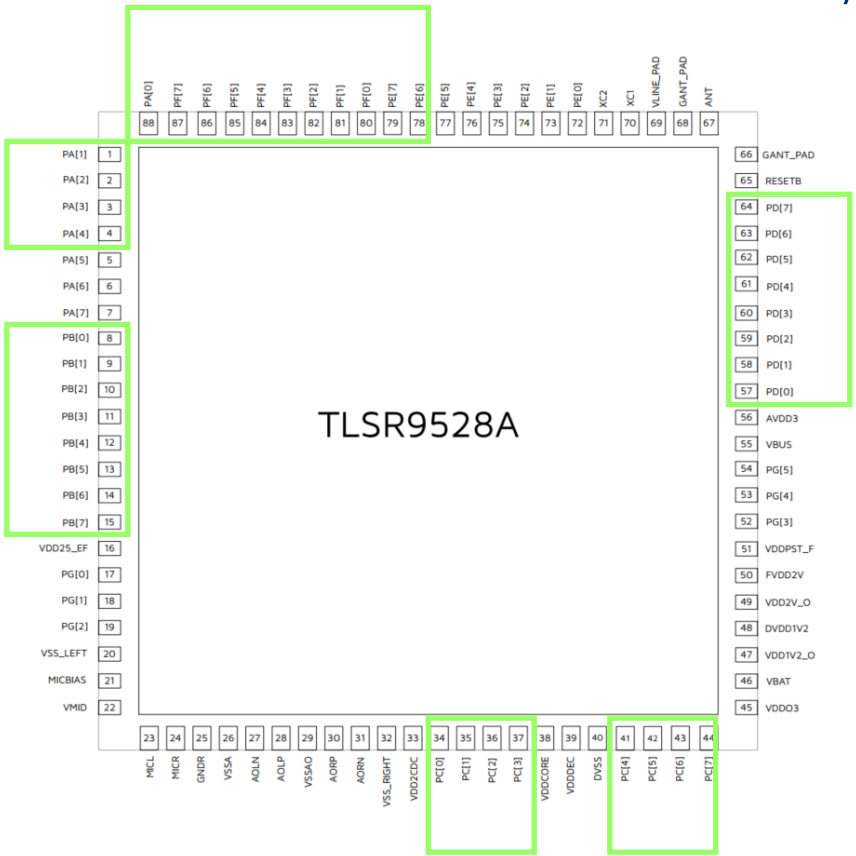
- A 4th-order LC filter is used for matching to pass certification, the values of which are flexibly adjustable corresponding to the layout. Here is the matching method.
  - Firstly, use VNA (Vector Network Analyzer) to do RX matching.
    - Customers must power on DUT, and use the EMI tool(provided by Telink) to configure the chip into RX mode, then tune RX matching.
  - After the RX test is finished, SA (Spectrum Analyzer) should be used to check the TX harmonic.
    - If harmonics do not meet the requirements, re-do RX matching. Use the VNA to adjust the component value to meet the impedance matching requirements, and then check the TX harmonic again.
- Combined with RF match tuning, the use of shield will make certification very easy.
- Telink TLSR9528A development board has passed FCC certification.
  - FCCID: OEOTLSR9528ADK88D

Pin layout – GPIO



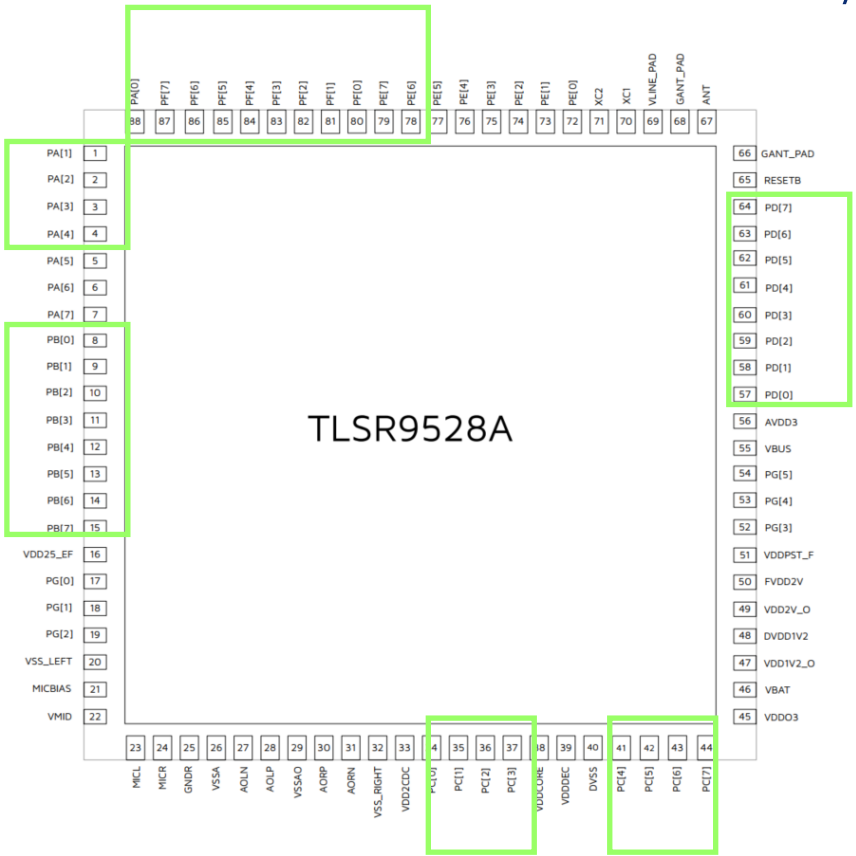
- All GPIO pins have configurable pull-up resistors and pull-down resistors.
  - Pull-up resistor: 10K/1M
  - Pull-down resistor: 100K
- All GPIO pins can be independently configured as high-level/low-level wakeup sources.
- Two kinds of driving strength:
  - PA[5:7], PE[0:1], PC[0:7], PD[0:7],PE[4:7] : maximum=8mA, minimum=4mA
  - Other GPIOs: maximum=4mA, minimum=2mA
  - Notes: the strength is weak when vddo3 is set as 1V8

Pin layout – PWM



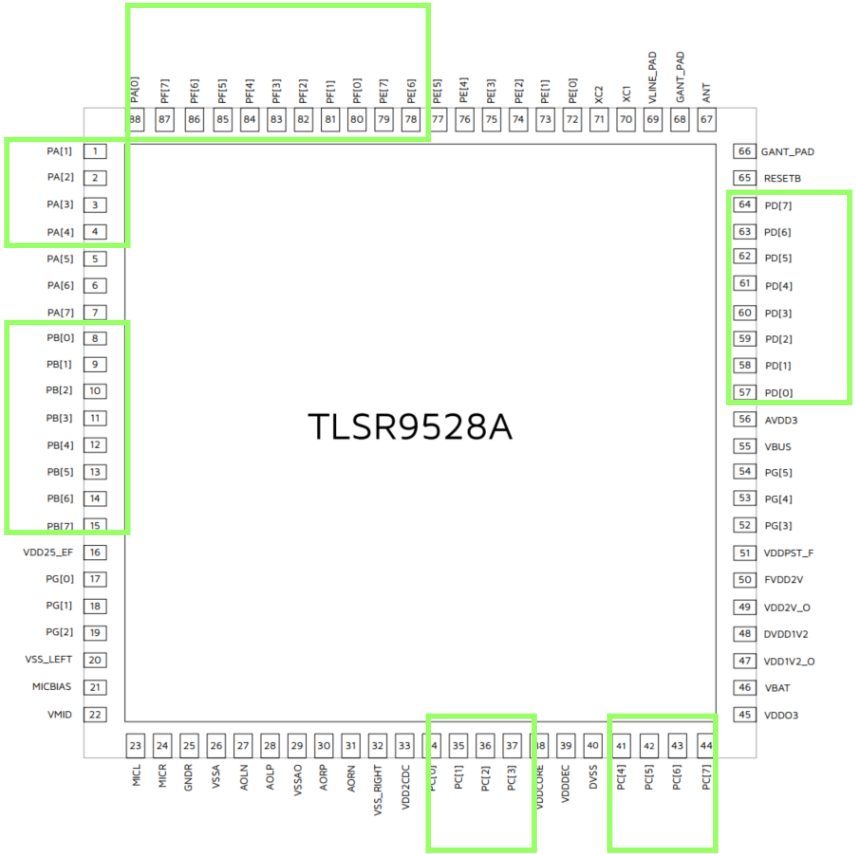
- Supports 6-channel PWM (Pulse-Width-Modulation) output. Each PWM#n (n=0~5) has its corresponding inverted output at PWM#n_N pin
- PWM0 supports five modes, including Continuous mode (normal mode, default), Counting mode, IR mode, IR FIFO mode, IR DMA FIFO mode. PWM1~PWM5 only support Continuous mode.
- Free configuration of any IO as PWM except PA5 to PA7, PE0 to PE5, and PG0 to PG5.

Pin layout – UART



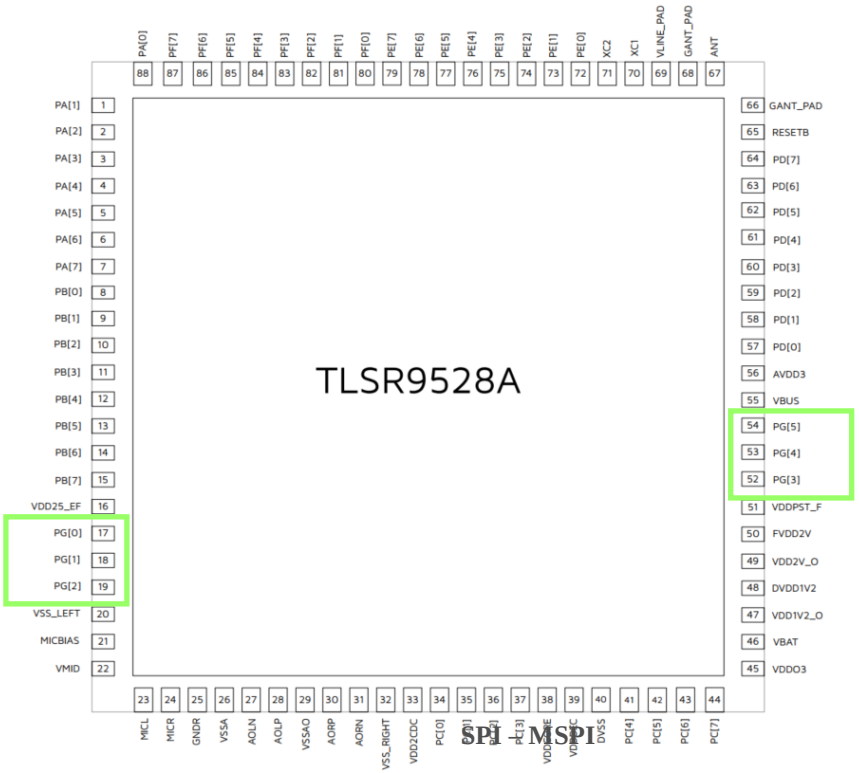
- Supports general UART interface and 7816 UART interface.
- Two groups of UART are supported: UART0 and UART1.
- Free configuration of any IO as UART except PA5 to PA7, PE0 to PE5, and PG0 to PG5

Pin layout – I2C



- Support two hardware I2C interfaces, I2C0 and I2C1
- Support I2C Master or Slave mode
- SCK/SDA of I2C0/1: Free configuration of any IO except PA5 to PA7, PE0 to PE5, and PG0 to PG5

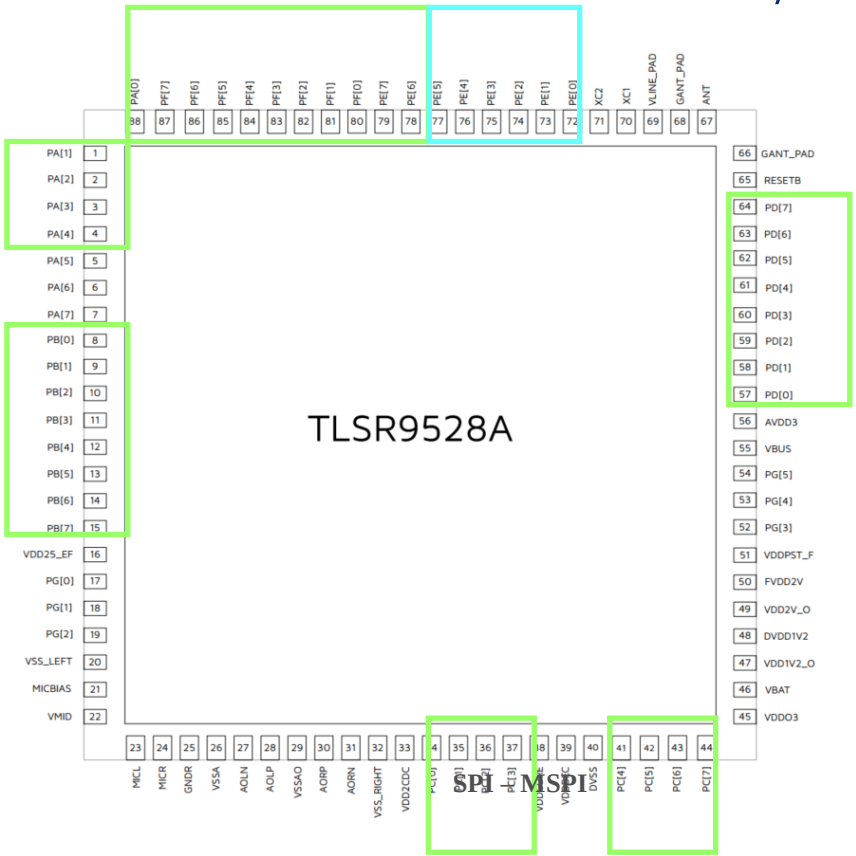
Pin layout – SPI : Part A



SPI – MSPI

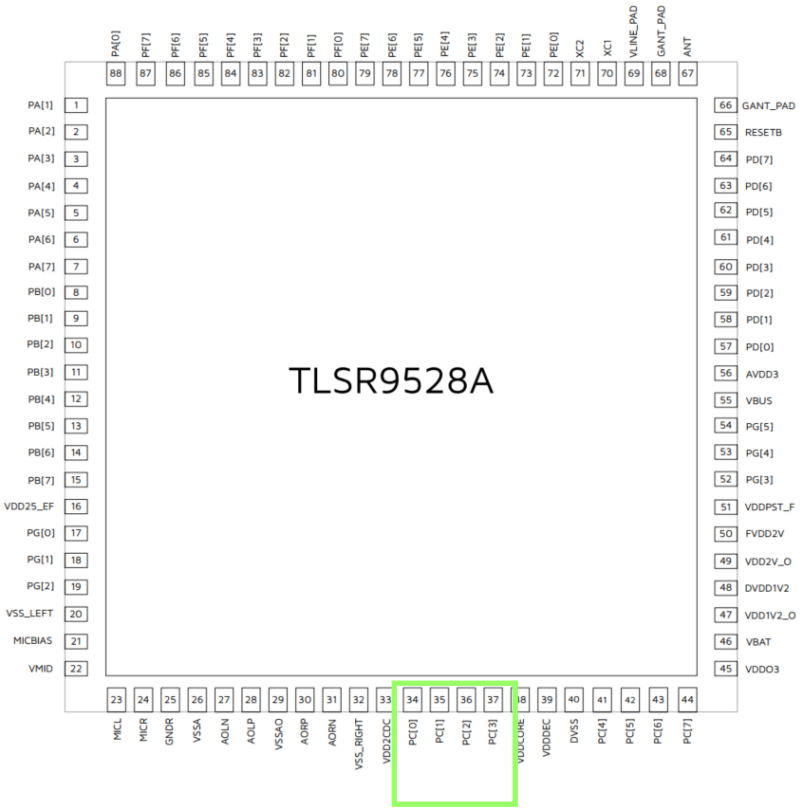
- Support MSPI/GSPI/LSPI/SSPI four SPI interfaces
- Rate support
  - MSPI: Single-line fastest rate to 64Mbps
  - GSPI: Single-line fastest rate to 48Mbps
  - LSPI: Single-line fastest rate to 48Mbps
  - SSPI: Single-line fastest rate to 24Mbps
- SPI – MSPI
  - MSPI connected to nor-Flash
    - MOSI: PG0
    - CK: PG1
    - IO3:PG2
    - CN: PG3
    - MISO: PG4
    - IO2:PG5

Pin layout – SPI : Part B



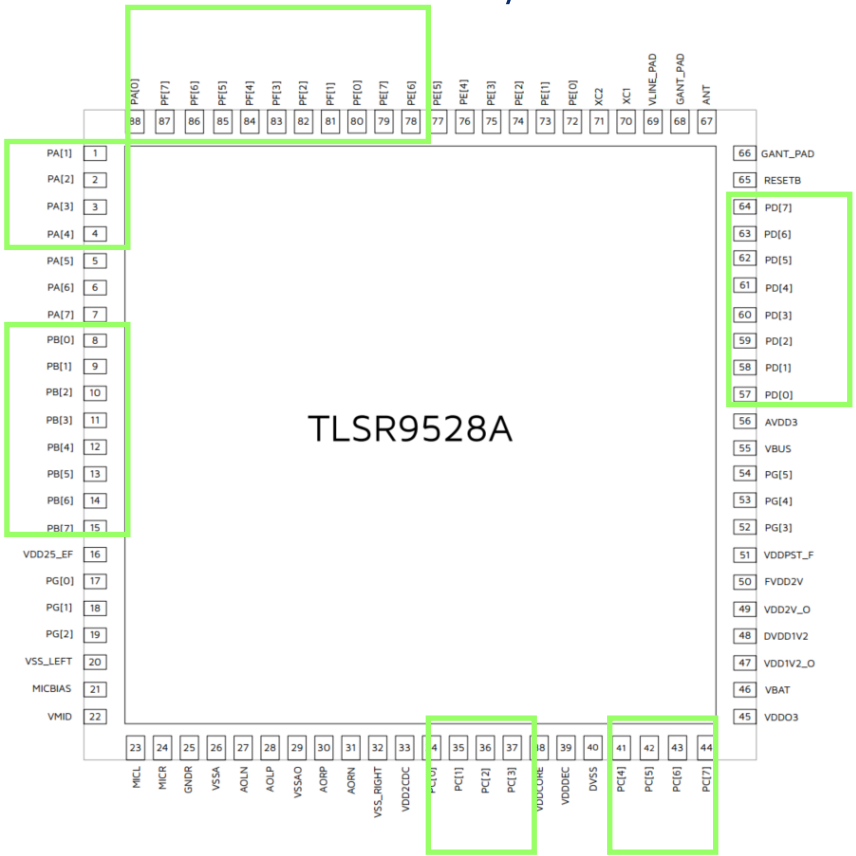
- SPI – GSPI
  - GSPI is a high-speed application, which can connect with PSRAM or NAND, support master or slave mode
    - Free configuration of any IO as GSPI except PA5 to PA7, PE0 to PE5, and PG0 to PG5
- SPI – LSPI
  - LSPI can be connected to LCD and supports master or slave mode
    - CN: PE0
    - CK: PE1
    - MOSI:PE2
    - MISO:PE3
    - IO2:PE4
    - IO3:PE5

Pin layout – SPI : Part C



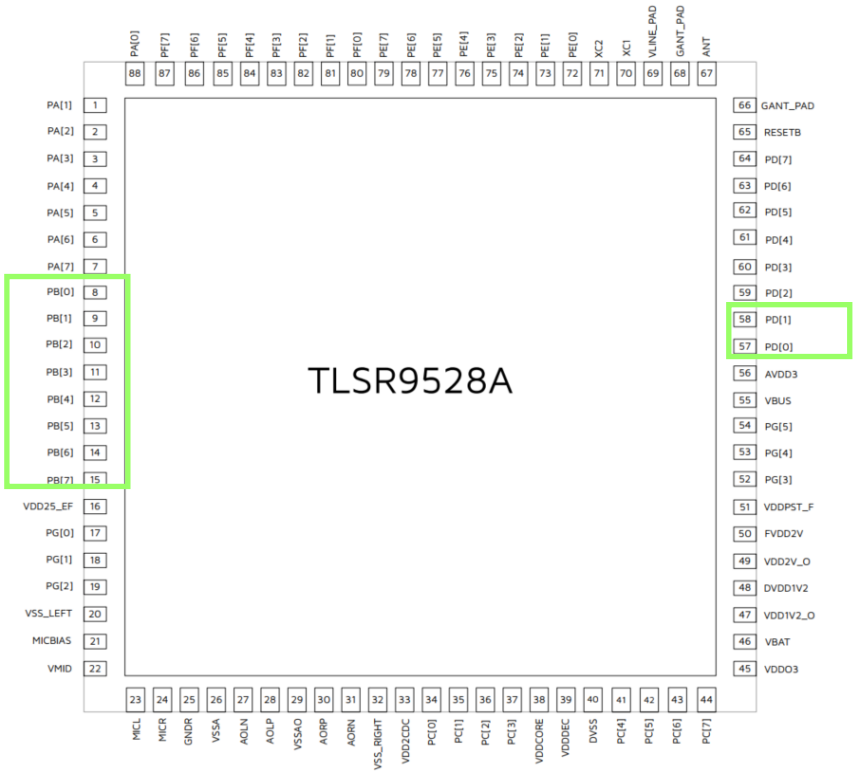
- SPI – SSPI
  - SSPI only support slave mode
    - CN:PC0
    - CK:PC1
    - SI:PC2
    - SO:PC3

Pin layout – RF front-end & Antenna Select Pins



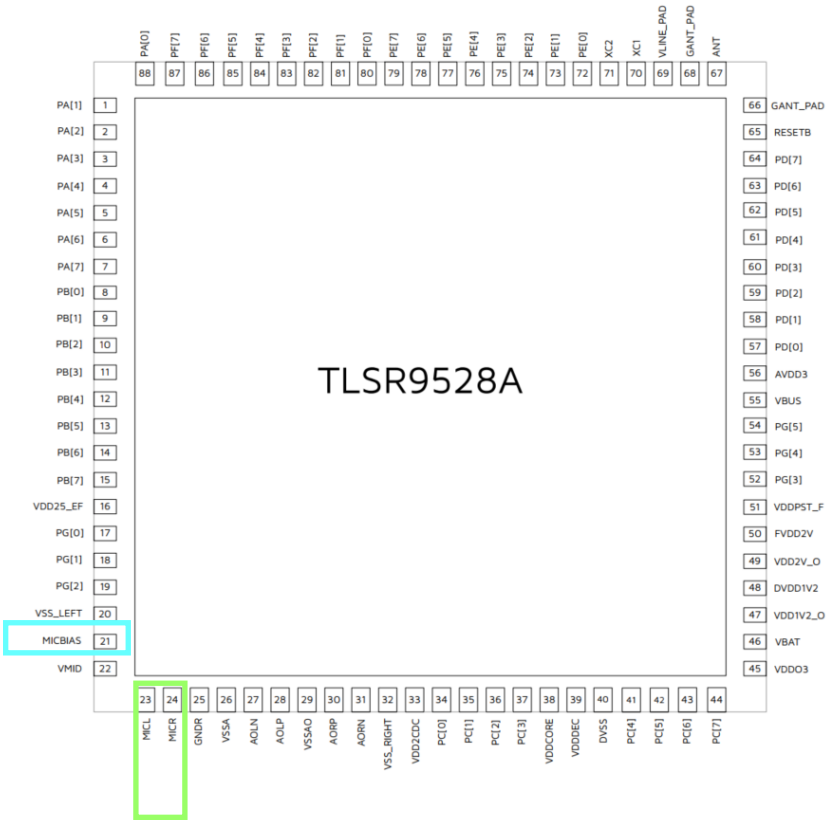
- External RF front-end Pins:
  - TXCYC is used to control the PA (Power Amplifier) of the external RF front end.
  - RXCYC is used to control the LNA of the external RF front end.
  - Free configuration of any IO as TXCYC/RXCYC except PA5 to PA7, PE0 to PE5, and PG0 to PG5
- Antenna Select Pins:
  - One group of SEL<0:3> is used to select one of up to sixteen external antennas. The selected antenna channel is connected to the RF_IO pin.
  - Free configuration of any IO as ATSELx except PA5 to PA7, PE0 to PE5, and PG0 to PG5

Pin layout – ADC Pins



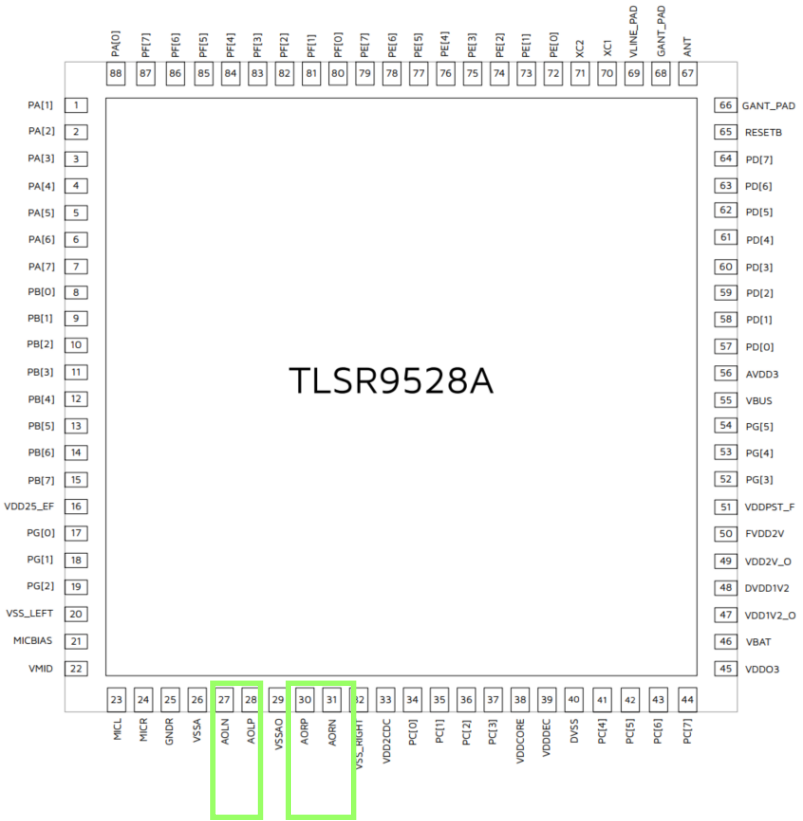
- ADC:
  - Supports up to 9 ADC pins, including PB1~PB7, PD0~PD1.
- Voltage detection:
  - VBAT channel detection: Directly detect the voltage on the VBAT pin
    - When vddo3 is 3.3V, detect range is 1.9V~4.3V
    - When vddo3 is 1.8V, not support VBAT channel detection
  - ADC pins detection
    - When vddo3 is 3.3V, resistor divider ratio 3/4(500K/1.5M(to GND))
    - When vddo3 is 1.8V, resistor divider ratio 1/3(1M/500K(to GND))

Pin layout – Audio Part: Part A



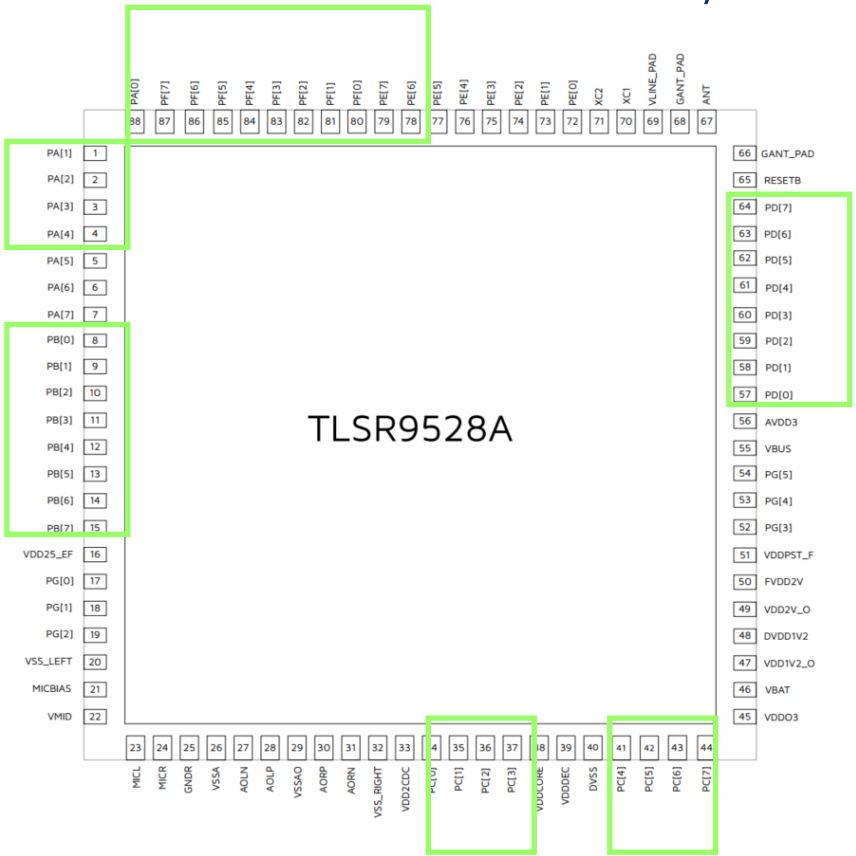
- Embedded Audio Codec:
  - Audio input path - AMIC:
    - Supports 2 channels, only single mode.
      - PIN23(MICL) are channel 1, higher priority.
      - PIN24(MICR) are channel 2.
    - PIN21 (MICBIAS) is the microphone power supply pin.

Pin layout – Audio Part: Part B



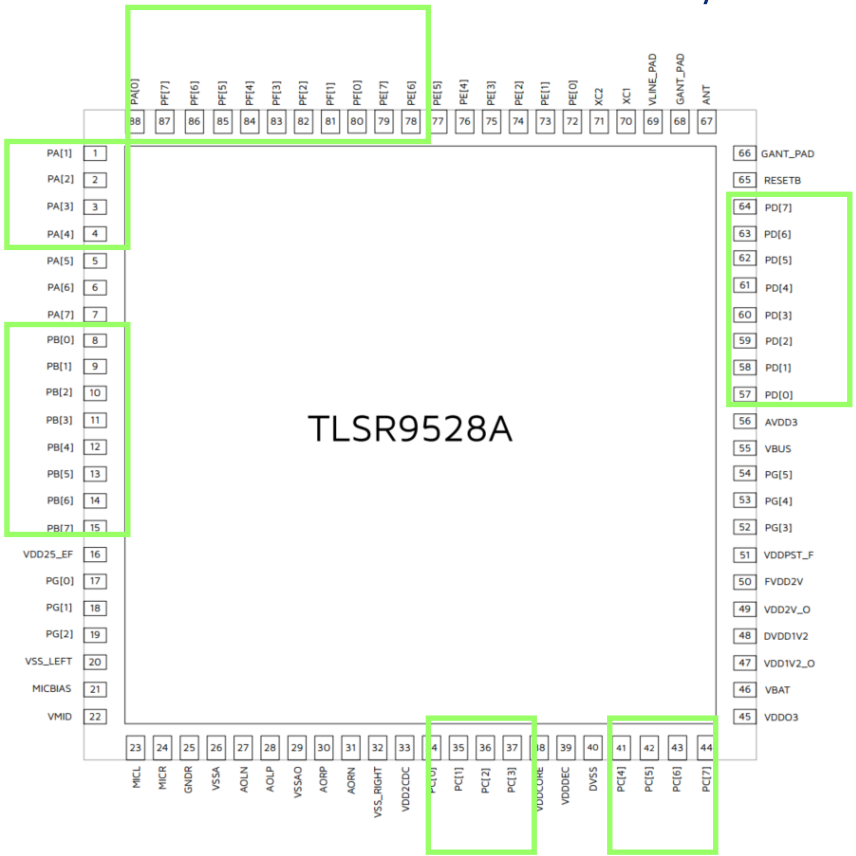
- Embedded Audio Codec:
  - Audio output path:
    - Supports 2 channels, differential mode.
      - PIN27(AOLN)/PIN28(AOLP) are L channel.
      - PIN30(AORP)/PIN31(AORN) are R channel.
    - For headset applications, support 16ohm and 32ohm speakers.
    - For watch applications, need to add an audio PA.
    - Single-end output is not recommended
      - There is a DC bias on the single-end signal line, and a DC isolation capacitor needs to be added to connect to the speaker.
      - The voltage amplitude of the single-end output signal is low, which is half of the differential output.

Pin layout – Audio Part: Part C



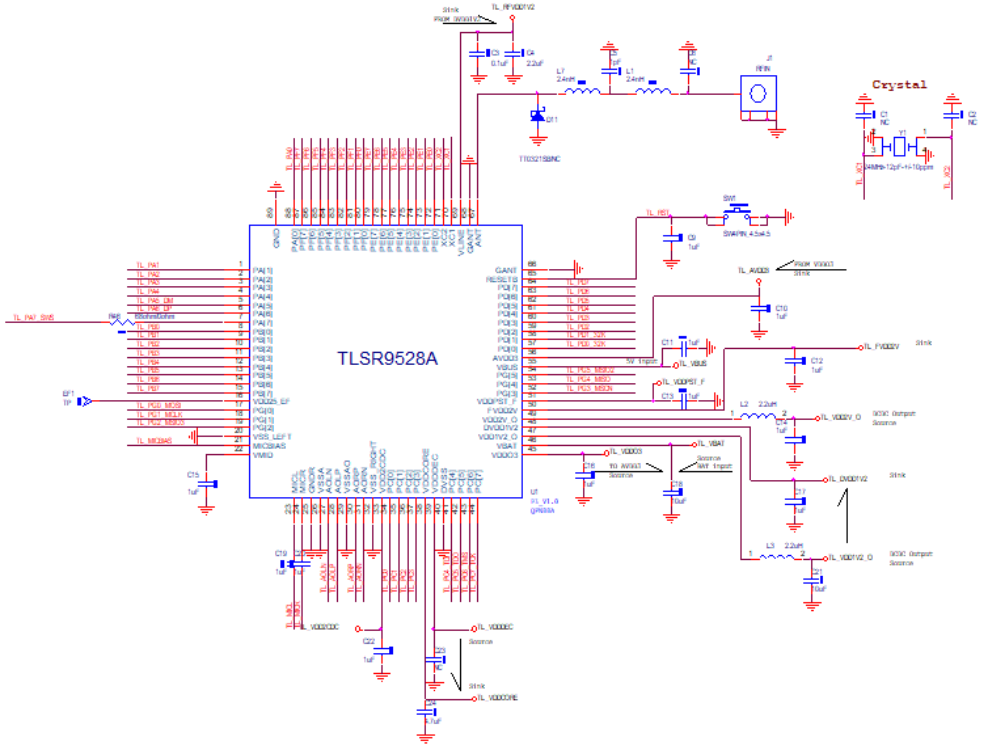
- DMIC:
  - Supports two digital microphones (DMIC0 and DMIC1)
    - DMIC0 – Data/Clk0:
      - Free configuration of any IO as Data/Clk0 except PA5 to PA7, PE0 to PE5, and PG0 to PG5
    - DMIC1 – Data/Clk1:
      - Free configuration of any IO as Data/Clk1 except PA5 to PA7, PE0 to PE5, and PG0 to PG5

Pin layout – Audio Part: Part D



- I2S interface:
  - Supports two I2S interfaces (I2S0 and I2S1)
  - I2S PINs
    - When working in 5-wires mode,
      - bit clk
      - output frame clk
      - output data
      - input frame clk
      - input data
    - When working in 4-wires mode,
      - bit clk
      - output frame clk
      - output data
      - input data
  - I2S pins can be configured in any combination except for PA5 to PA7, PE0 to PE5, and PG0 to PG5

Reference Design

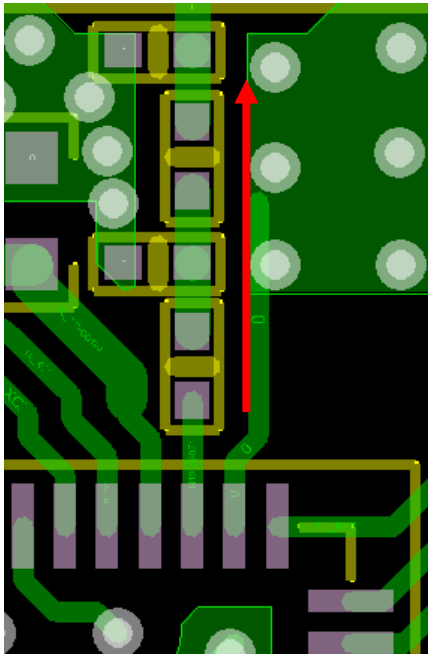


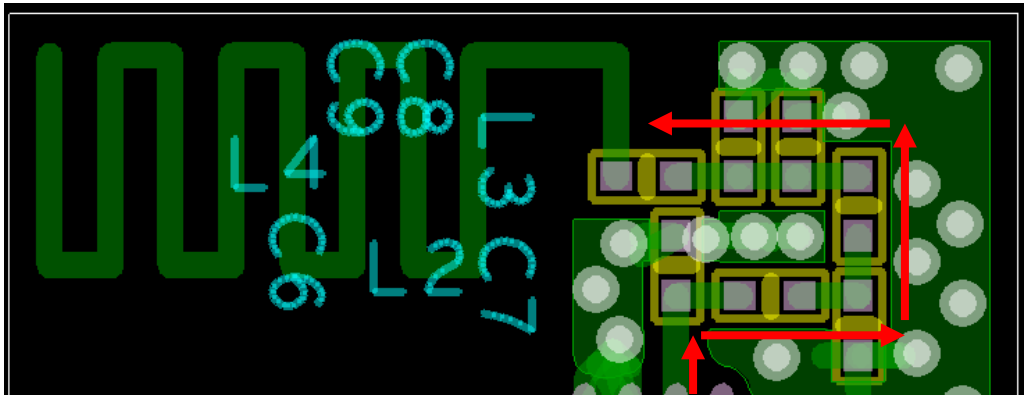
PIN ID	PIN Name	Capcitance	Inductance
22	VMID	1uF	
33	VDD2CDC	1uF	
39	VDDDEC	NC	
38	VDDCORE	4.7uF	
45	VDDO3	1uF	
46	VBAT	10uF	
47	VDD1V2_O	10uF	2.2uH
48	DVDD1V2	1uF	
49	VDD2V_O	1uF	2.2uH
50	FVDD2V	1uF	
51	VDDPST_F	1uF	
56	AVDD3	1uF	
69	VLINE	0.1uF+2.2uF	

PCB Design Guideline

RF layout

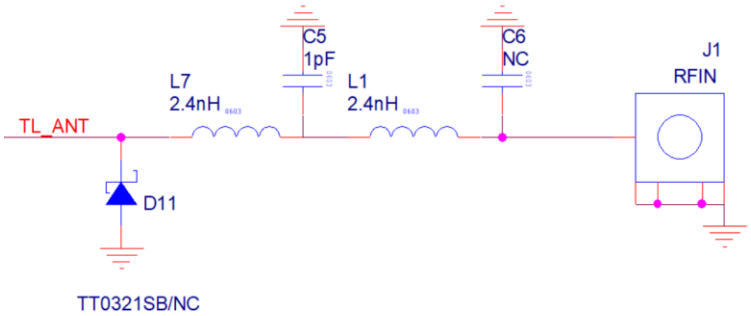
- The components on the RF path MUST be placed one by one. and they MUST be placed close to each other, no stub.
- It the area is not enough, can fold it, but MUST use ground and via to shield RF trace.



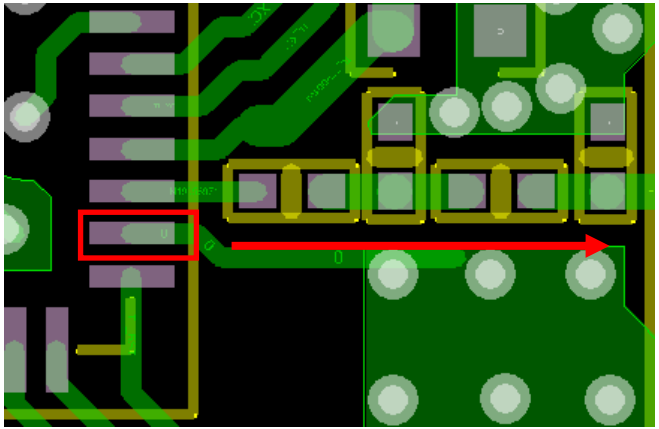


GANT PAD

- GANT pad, which is in the red box, MUST be connected out. And CAN`T connect it to E-PAD directly.
- Recommend to use 4th-order filter to pass certification.

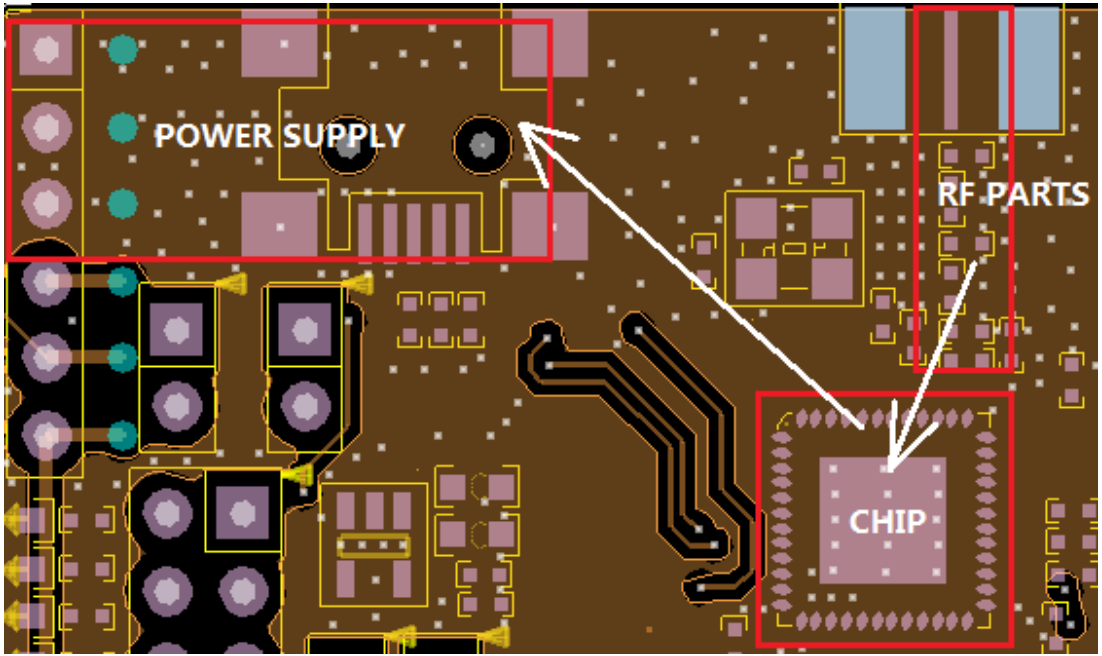


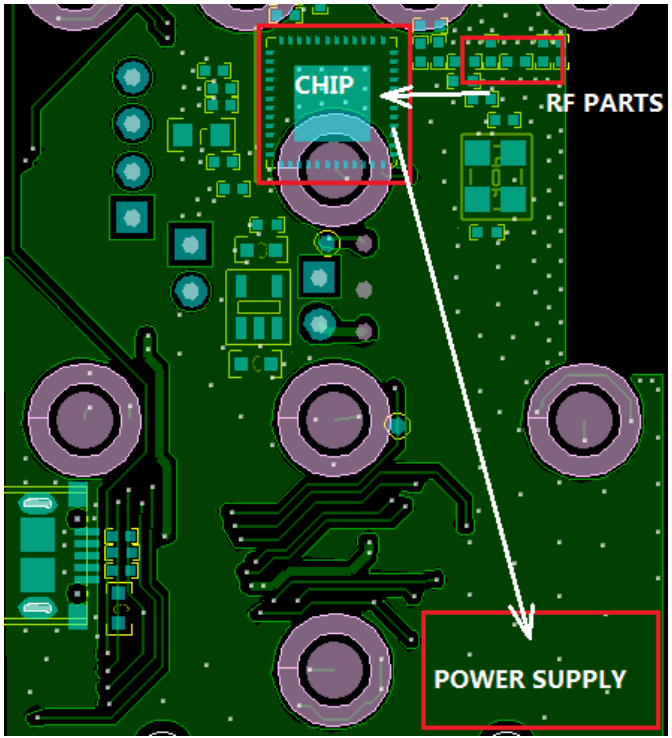
Note: The above values are just for reference.



Solid Ground Plane

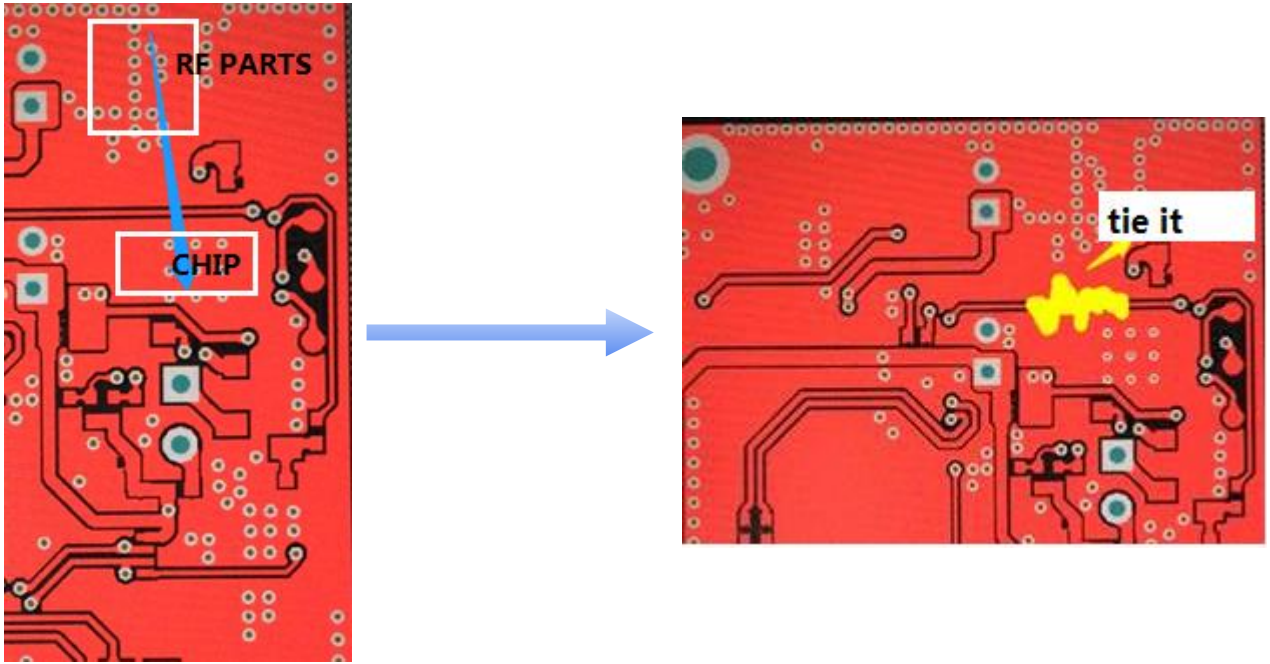
- The ground plane MUST be wide, solid. The ground plane from power supply to chip, then at last to RF parts MUST be solid.
- A good examples are as below.





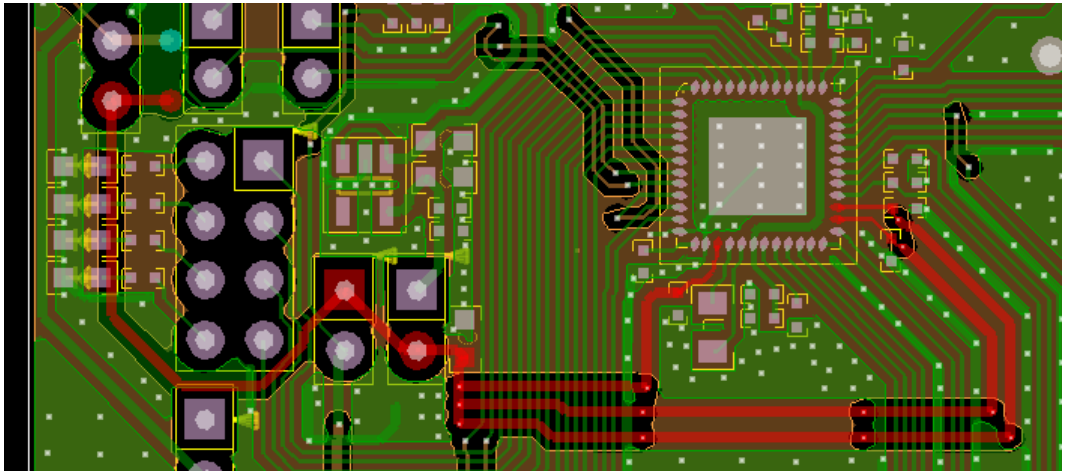
Solid Ground Plane(Cont)

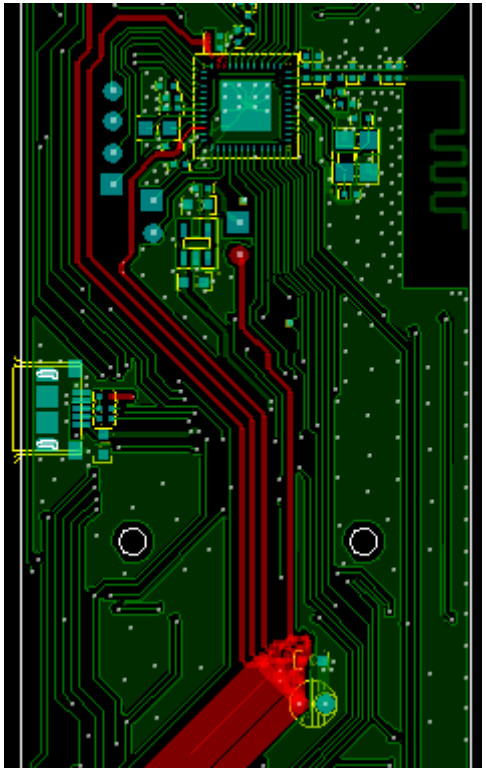
- A bad example is as below.
  - Ground plane between RF parts and chip is cut off, the rx performance is greatly affected.
  - Tie them together, the RX performance matches the data on the datasheet.



Star connection

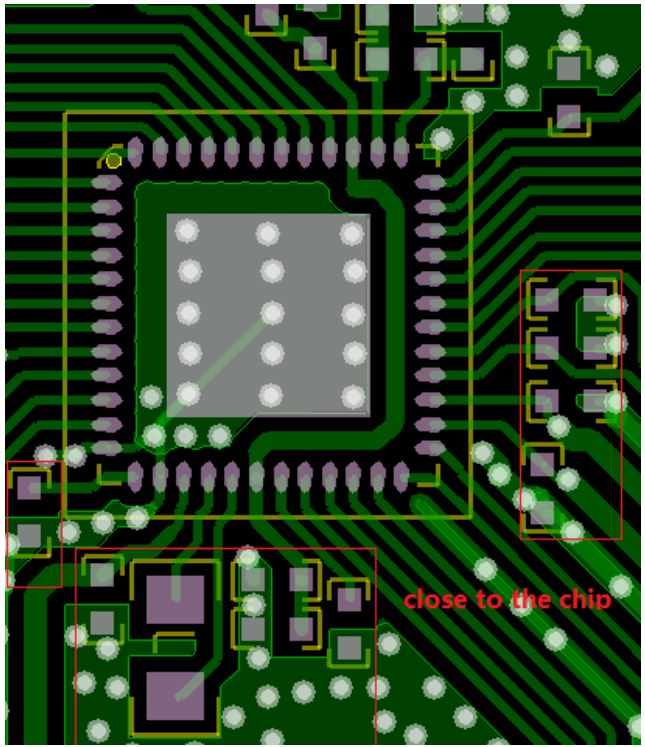
- Power supply should be connected in star-type connection.
  - If there is no audio function, can connect them together.

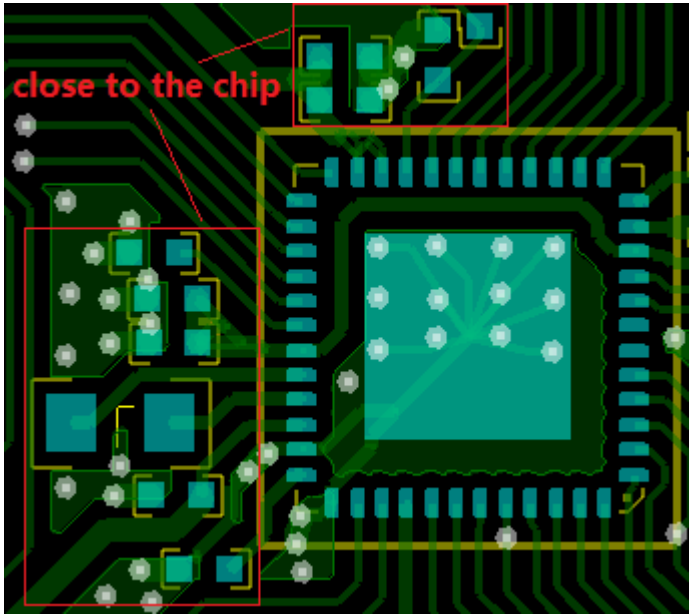




Decoupling capacitor

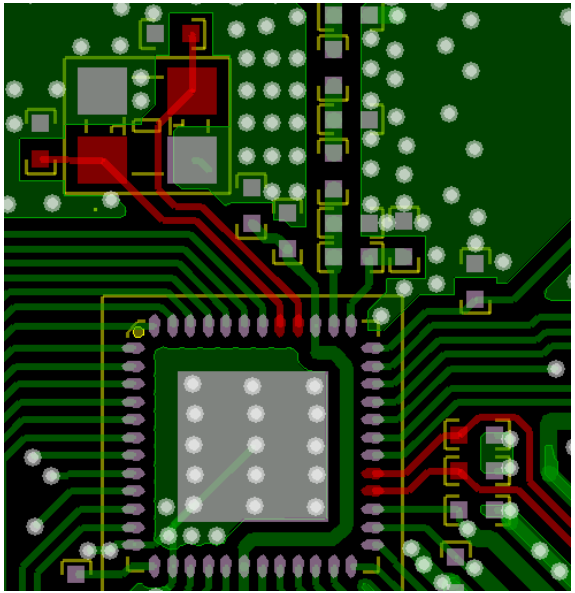
- Decoupling capacitors MUST be placed close to power pins.

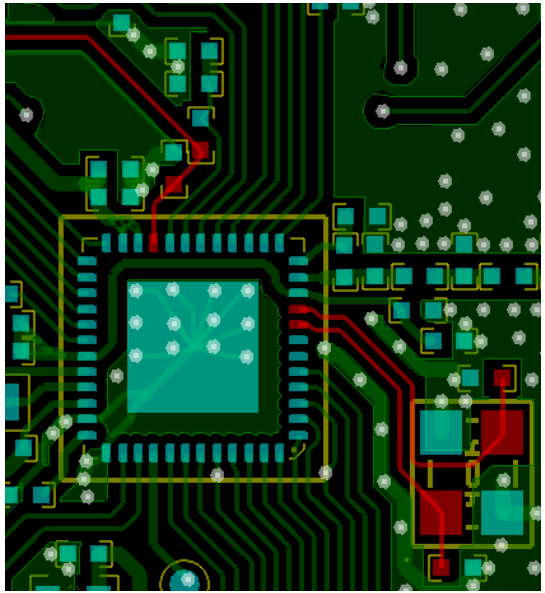


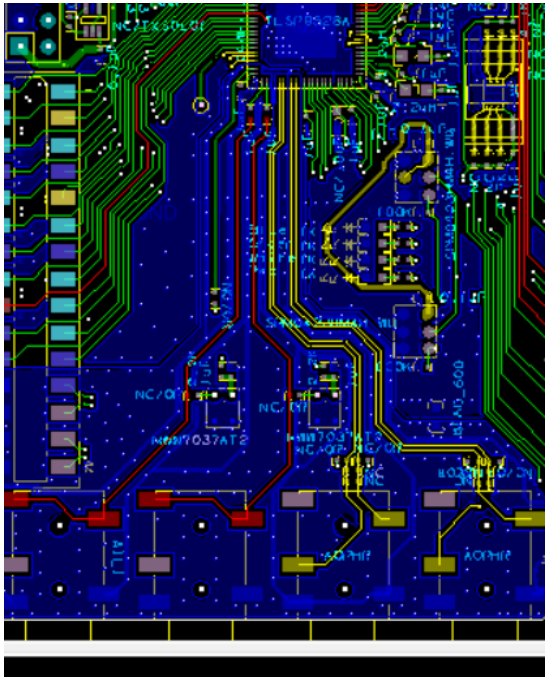


Key traces

- To avoid EMI issue, some important parts such as crystal, audio trace, mic trace and usb trace MUST be shielded by GND and via.

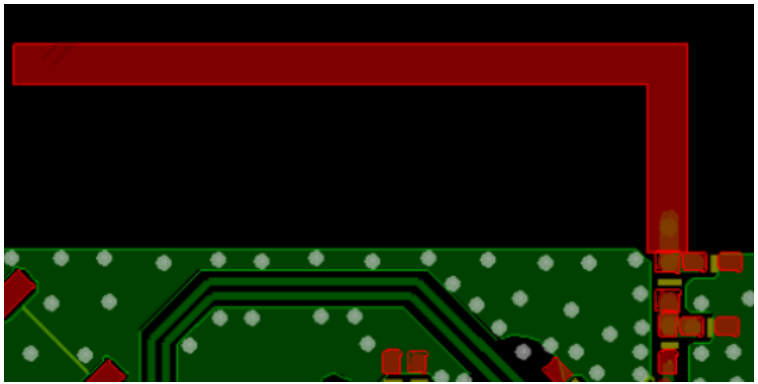






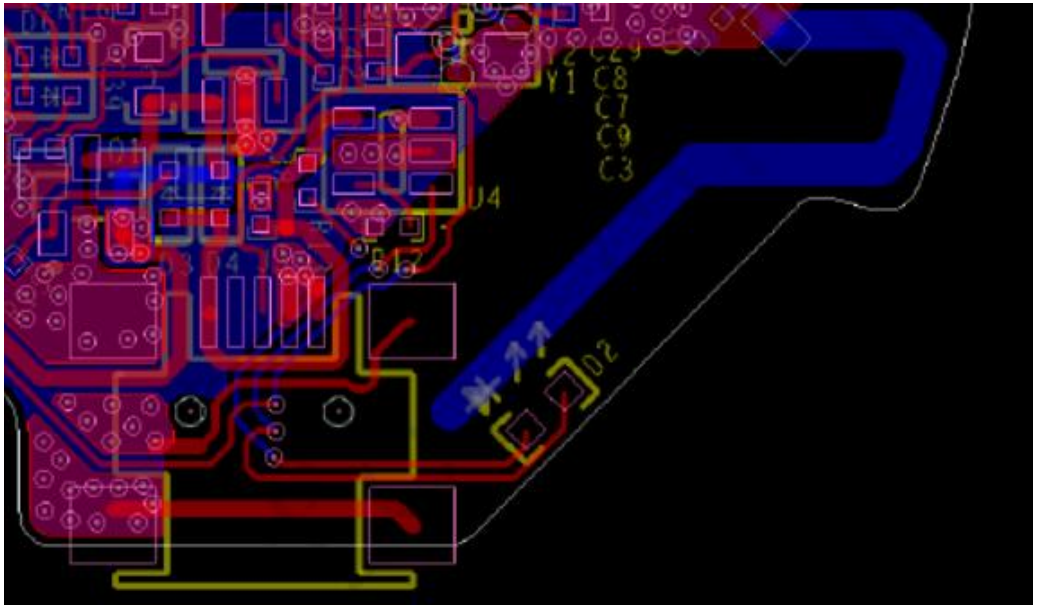
Antenna – common requirement

- Antenna trace width shouldn`t be too narrow in order to decrease loss.
- Line width should be 0.5mm or above, generally it`s recommended to be 0.5mm or 1mm.
- Top and bottom of antenna location should not be covered by GND.
- The distance between antenna and GND should be 3mm or above.
- Generally antenna length is 20mm~30mm. The smaller the GND is, the longer the antenna should be.



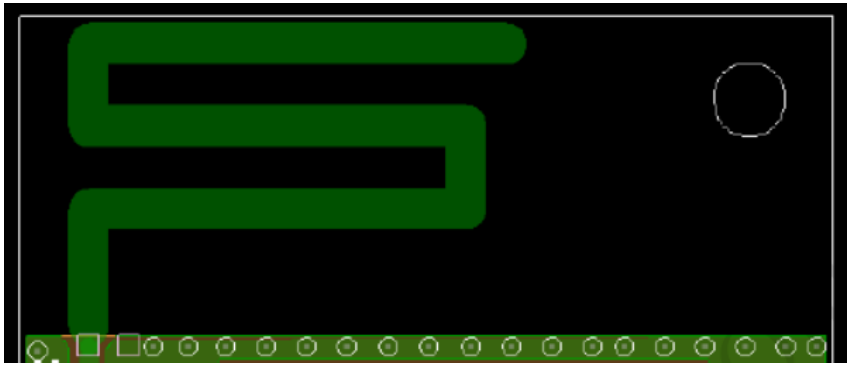
Antenna – keep away others

- Keep PCB antenna far away from metal, battery, or other components, such as 3mm or 5mm.
- A bad example is showed as below. The antenna is too close to USB connector.



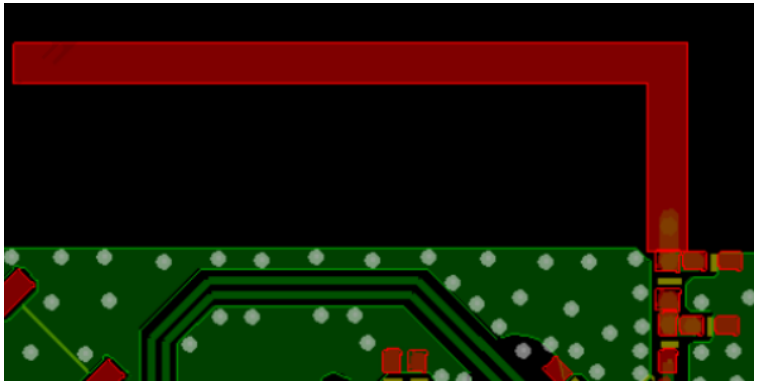
Antenna – don`t exposed to others

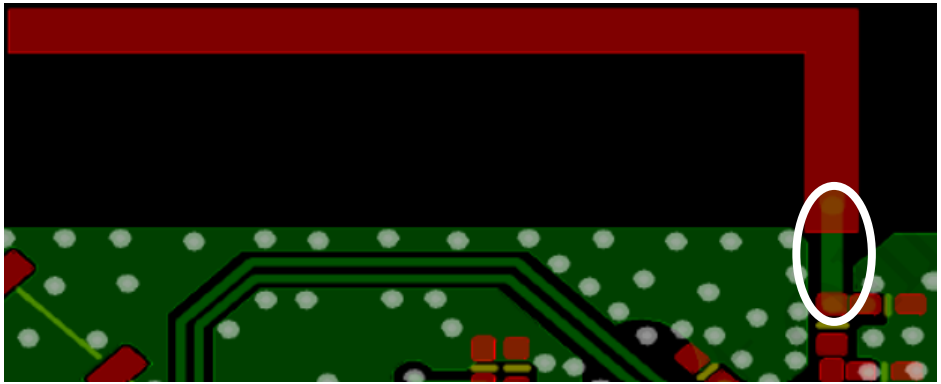
- There MUST be a row of via holes along the antenna on the side parallel to GND. Do not directly expose trace or pad to the antenna.
- The left is a good example. The right is a bad example.



Antenna – matching components

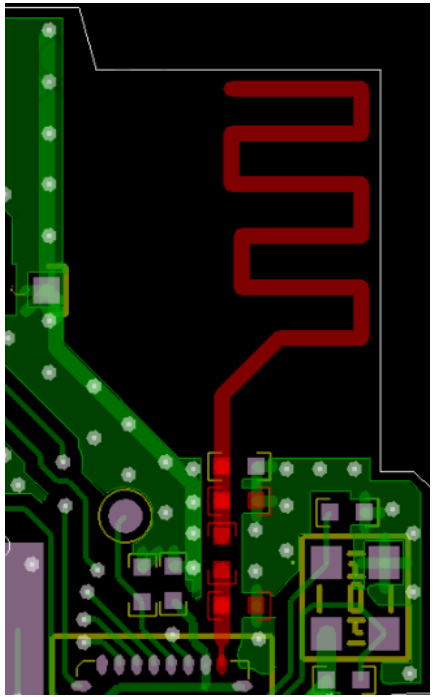
- Antenna matching components should be placed at the boundary of antenna and GND without shrink inward or expand outward.
- The left is a good example. The right is a bad example.

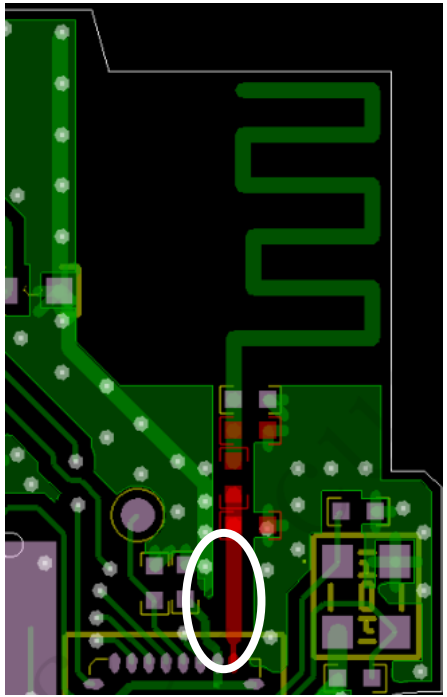




Antenna – impedance design

- The RF line to the antenna port should be short. If RF trace can`t be designed shortly, it must be designed as 50ohm micro-strip line.
- The left is a good example. The right is a bad example.

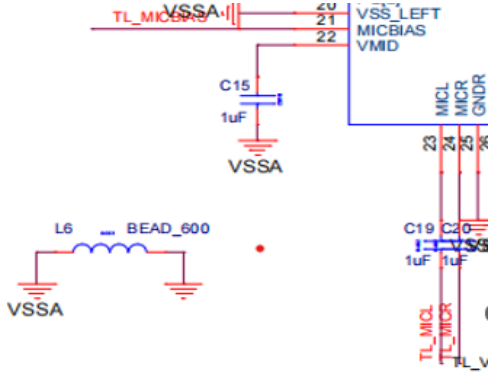




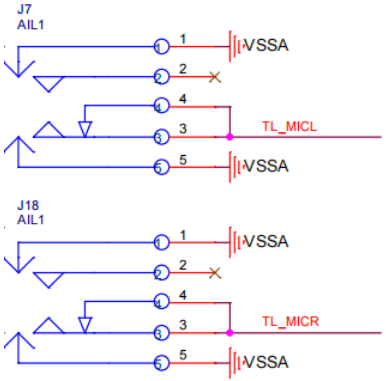
Audio Design Guideline

Audio Input – Codec

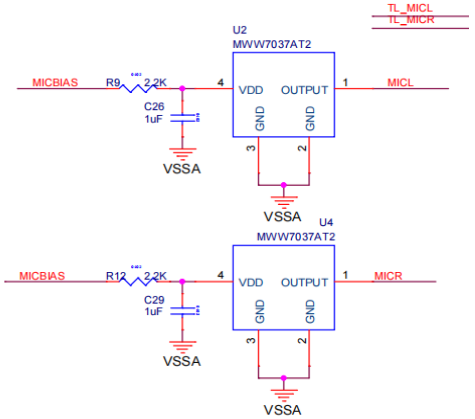
- Support two audio input channels, MIC_L has a higher priority.
- Only support single-ended inputs
  - Chip site: MICL or MICR series connected 1uF capacitor.
  - LINE_IN: This method can be connected to a single input 3.5 mm audio jack.
  - MEMS MIC: MICBIAS needs attention to add filtering.



Chip Site



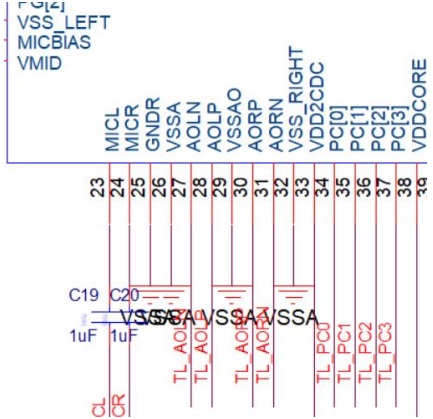
LINE_IN Connection

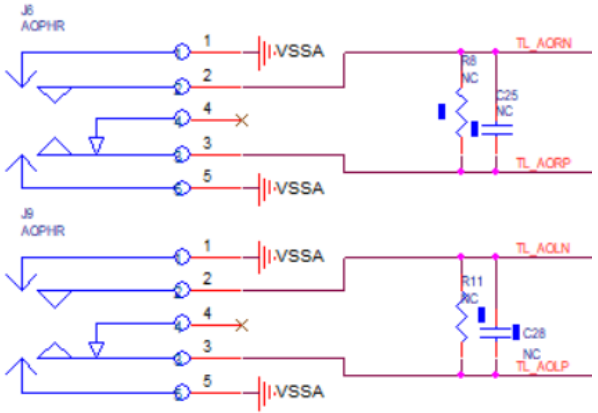


MEMS MIC connection

Audio Output – Codec

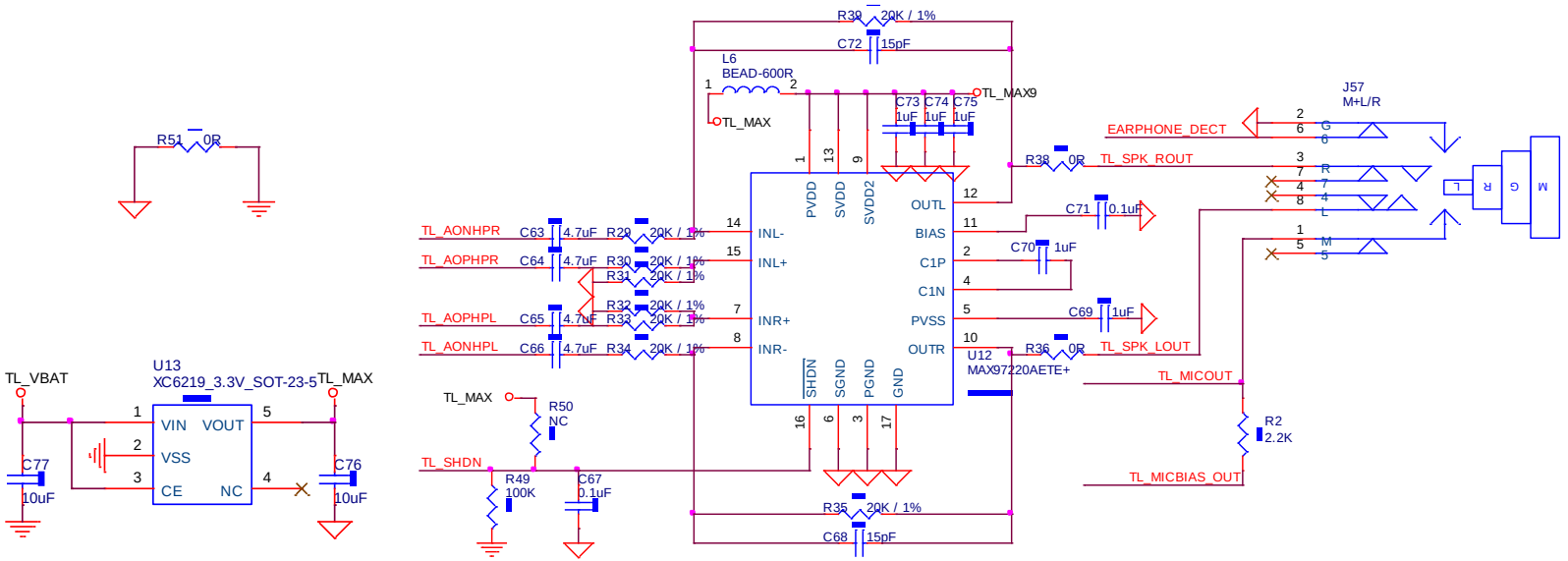
- Audio support stereo channel output, only support differential connection
  - AOLP and AOLN are the positive and negative poles of the audio left channel output.
  - AORP and AORN are the positive and negative poles of the audio right channel output.
  - The left and right channels are connected to the speakers, supporting 16ohm and 32ohm load.





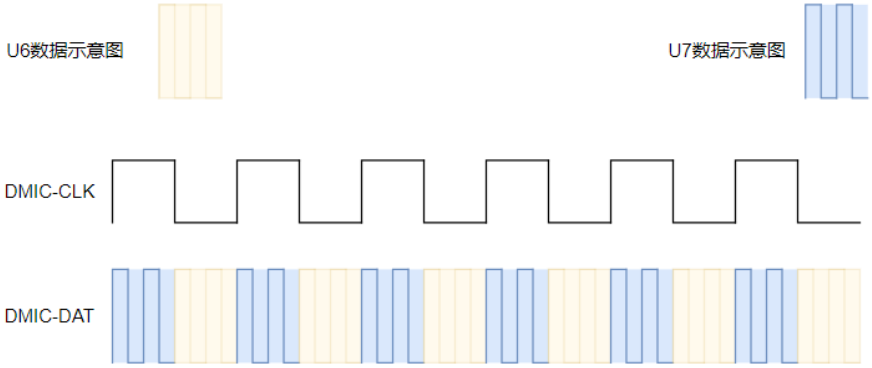
Audio Output – Codec

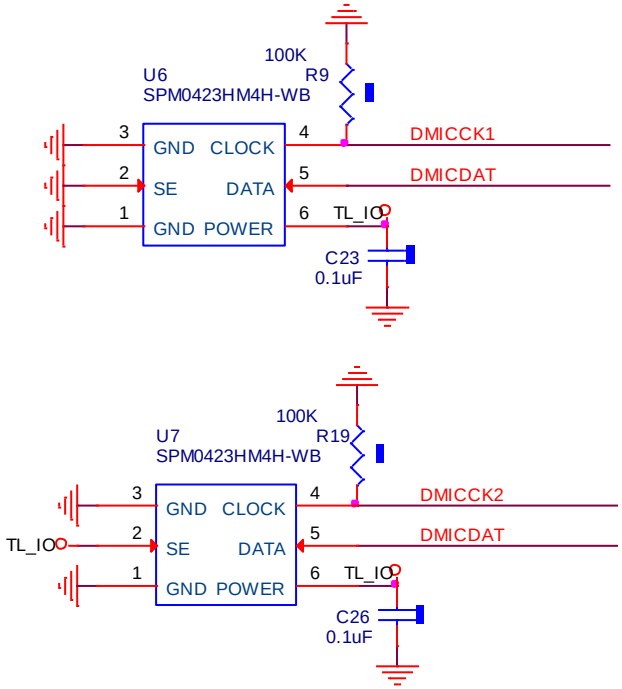
- Single-ended audio output, requires additional differential to single-ended chip
- Differential to single-ended part of the analog ground and chip ground with OR resistor for isolation.
- A LDO is set separately for the power supply of the differential to single-ended part, isolating the power supply from the chip power supply.



Audio Input – DMIC

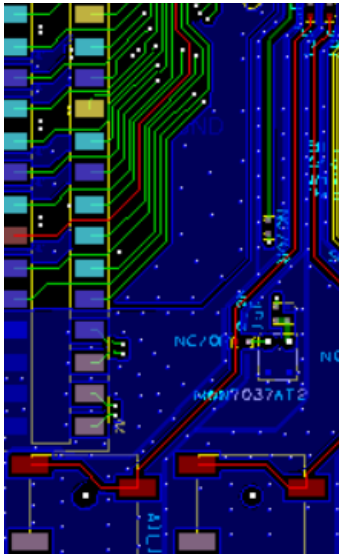
- Audio input path – DMIC:
  - Supports two digital microphone inputs.

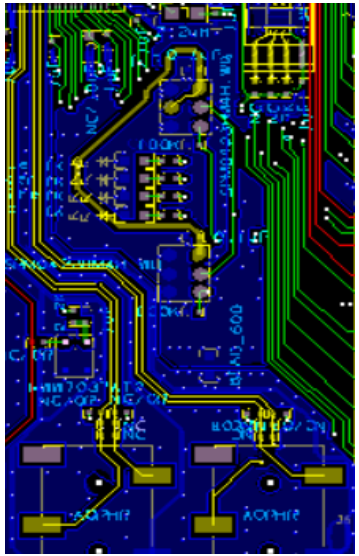




Audio – Layout Design

- Audio Input&Output:
  - Audio routing can't be parallel to the power line and high-speed signal lines, and as far away as possible, pay attention to crossover routing.
  - Audio alignment try not to change the layer over the hole.
  - Attention to the ground package treatment.





Change Logs

- 2023.03.20:
  - Initial version
- 2023.08.08:
  - Updated GPIO driver strength
- 2024.05.20:
  - Add “GANT PAD” slide
  - Add “ Reference Design ” slide
  - Correct some descriptions