Telink

Telink Semiconductor

B91 Hardware Design Guideline

2023-12

Scope

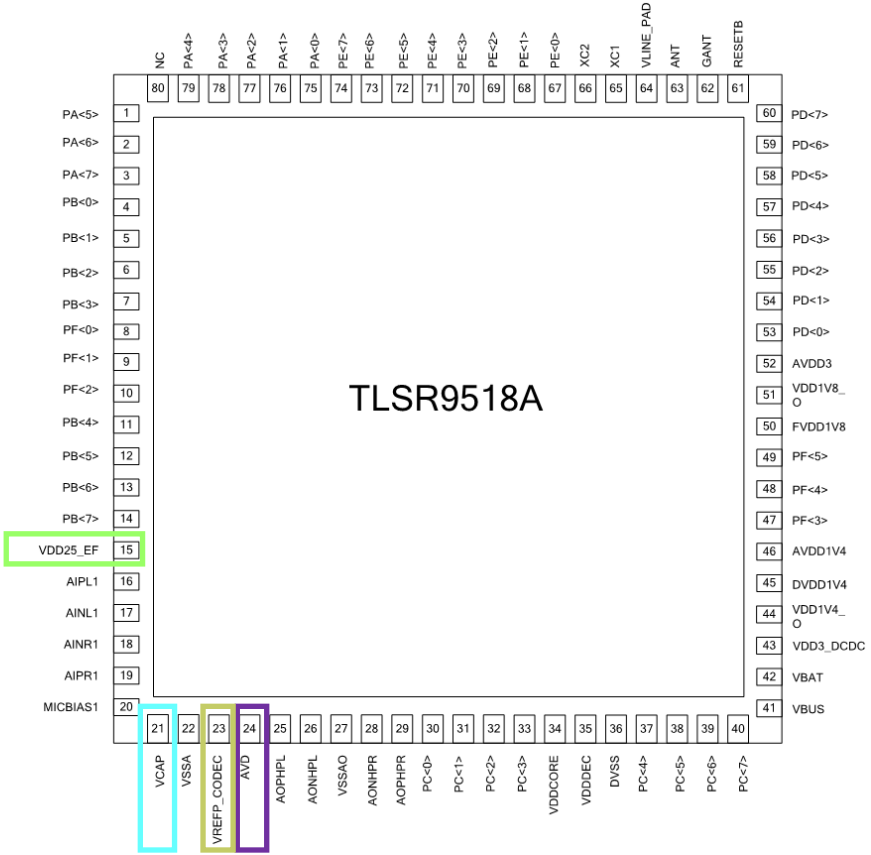
- Chip`s datasheet is the basic reference file of hardware design. This document will go through datasheet with hardware engineer and supplement some details. It will speed up projects after reading the document.
- Considering that the chip`s datasheet will be continuously updated, if there is any difference between this document and the chip`s datasheet, please refer to the latest version of the chip specifications.
- The version and link of the chip`s datasheet mentioned in this document are as follows:
  - DS_TLSR9518-E15_Datasheet for Telink Multi-Standard Wireless SoC TLSR9518
    - http://wiki.telink-semi.cn/wiki/chip-series/TLSR9-Series/
- TLSR9518A is taken as an example to describe. And the content mentioned in the file applies to the B91 chipset serials.

Schematic Design Guideline

Reference Schematic

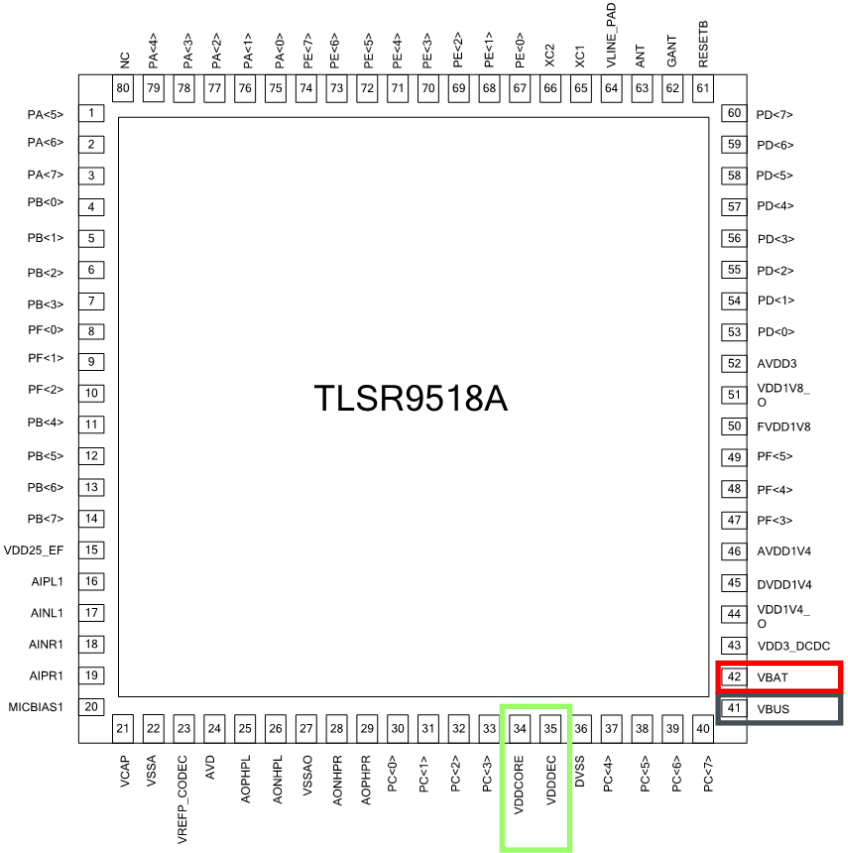
- Reference Schematic:
  - Refer to chapter 3 (reference design).
  - TLSR9518B`s reference design are listed here.
    - Schematic and BOM are listed together.
  - The schematic is the design of minimum core system
    - Easy to copy into other designs.
    - Easy to count the cost at the stage of design-in.

Pin layout – Power Supplies : Part A



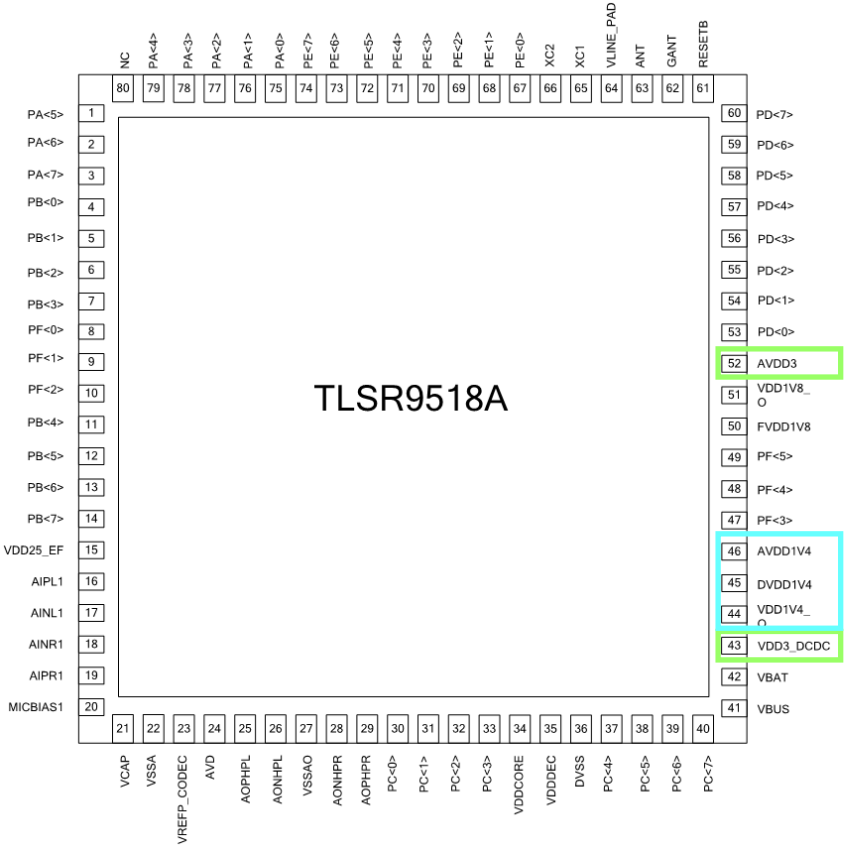
- PIN15(VDD25_EF):
  - Only packaged out on TLSR9518A which is used by E-fuse.
  - A decoupling capacitor, 1uF, is needed.
- PIN21(VCAP):
  - Related to embedded codec part in the chip.
  - A decoupling capacitor, 1uF, is needed.
- PIN23(VREFP_CODEC):
  - Related to embedded codec part in the chip.
  - A decoupling capacitor, 10uF, is needed.
- PIN24(AVD):
  - Related to embedded codec part in the chip.
  - PIN24(AVD) is the power supply of embedded codec that a decoupling capacitor, 1uF, is needed. Usually connected to 2.8V power source.

Pin layout – Power Supplies : Part B



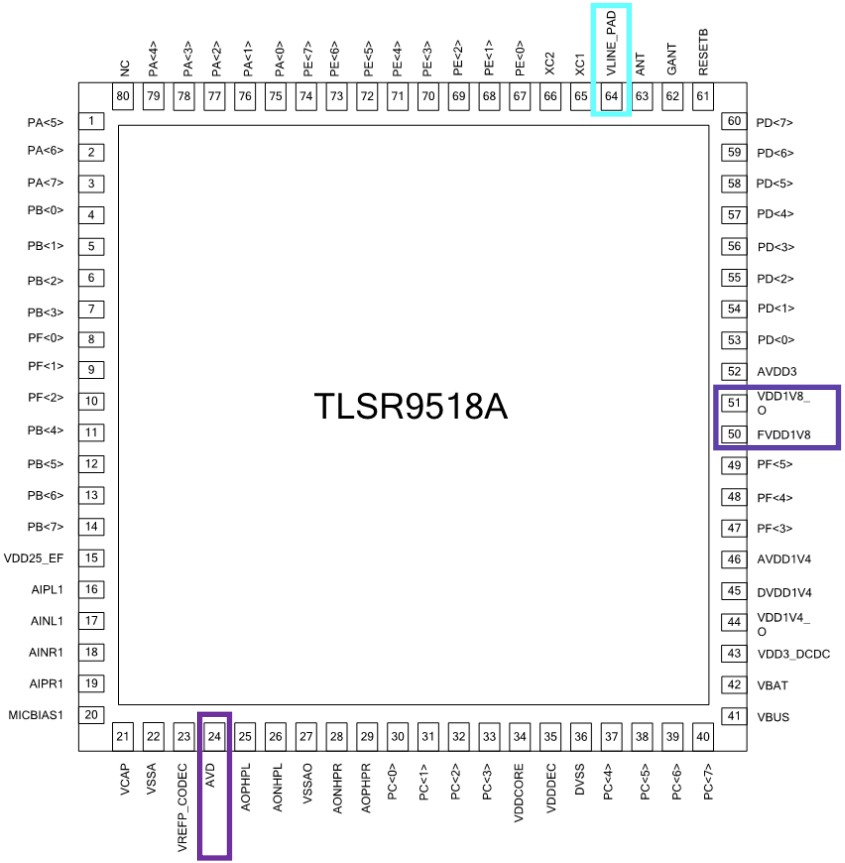
- PIN34(VDDCORE)/PIN35(VDDDEC):
  - Connected together. And a decoupling capacitor, 1uF, is needed.
- PIN41(VBUS) :
  - Only internal charger input. A decoupling capacitor, 1uF, is needed when charging Lion-battery.
  - When not using internal charger, don`t connect it to anything.
  - Recommend to use external charger for easy customizing.
  - Regardless of using internal or external charger, an OVP chip is recommended to used in a real application.
- PIN42(VBAT):
  - Battery positive terminal. A decoupling capacitor, 1uF, is needed.
  - Lion-battery positive terminal can be directly connected to the pin since voltage range is 1.8V~4.3V.
  - If USB VBUS(5V) is available in application, a external LDO or DCDC is recommended to use for converting USB VBUS(5V) to 3.8V for VBAT pin.

Pin layout – Power Supplies : Part C



- PIN43(VDD3_DCDC)/PIN52(AVDD3):
  - connected together. And a decoupling capacitor, 1uF, is needed.
  - Power supply for all GPIOs.
  - PIN43 is 3V3 Source, PIN52 is 3V3 Sink.
- PIN44(VDD1V4_O)/PIN45(DVDD1V4)/PIN46(AVDD1V4):
  - PIN44 is 1V4 DCDC Source, PIN46 is 1V4 LDO Source.
  - PIN45/PIN64 are 1V4 Sink.
  - LDO and DCDC mode are both supported. In real application, DCDC mode is suggested.
  - Some decoupling capacitors are needed.

Pin layout – Power Supplies : Part D



- PIN50(FVDD1V8)/PIN51(VDD1V8_O)/PIN24(AVD):
  - PIN50 is 1V8/2V8 LDO Source, PIN51 is 1V8/2V8 DCDC Source.
  - PIN24 is 1V8/2V8 Sink which is power supply of codec part.
  - LDO and DCDC mode are both supported. In real application, LDO mode is suggested. When using LDO mode, remove inductor and connected all the PINs together.
  - Some decoupling capacitors are needed.
- PIN64(VLINE_PAD):
  - Related to RF part in the chip, power supply for RF part.
  - Decoupling capacitor, 2.2uF&0.1uF, are needed.

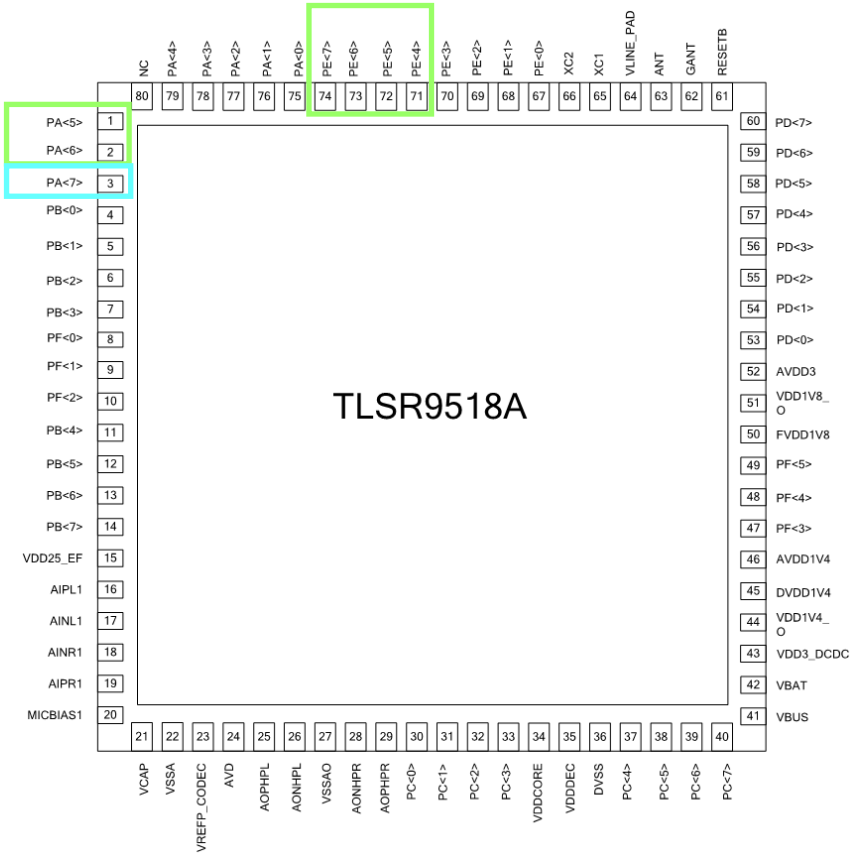
Pin layout – Power Supplies : Part E

- Description of the selection of DCDC inductor:
  - Both VDD1V4 and VDD1V8 support DCDC mode. An external 10uh inductor is needed in DCDC mode. To ensure the DCDC load capacity and DCDC efficiency, wire-wound inductors with low DCR, high-rated current and high Q value usually be selected.
  - The inductor for Telink's EVB is the LQH2HPN100MJRL (Murata), which has an efficiency greater than 80%. The specifications are as follows:

Inductor@ 1MHz	Brand	Model	Structure	Package /inch	DCR/Ω	Self-frequency	Rated current(mA)
10uH	muRata	LQH2HPN100MJRL	Wire	1008	0.38±20%	30MHz	490

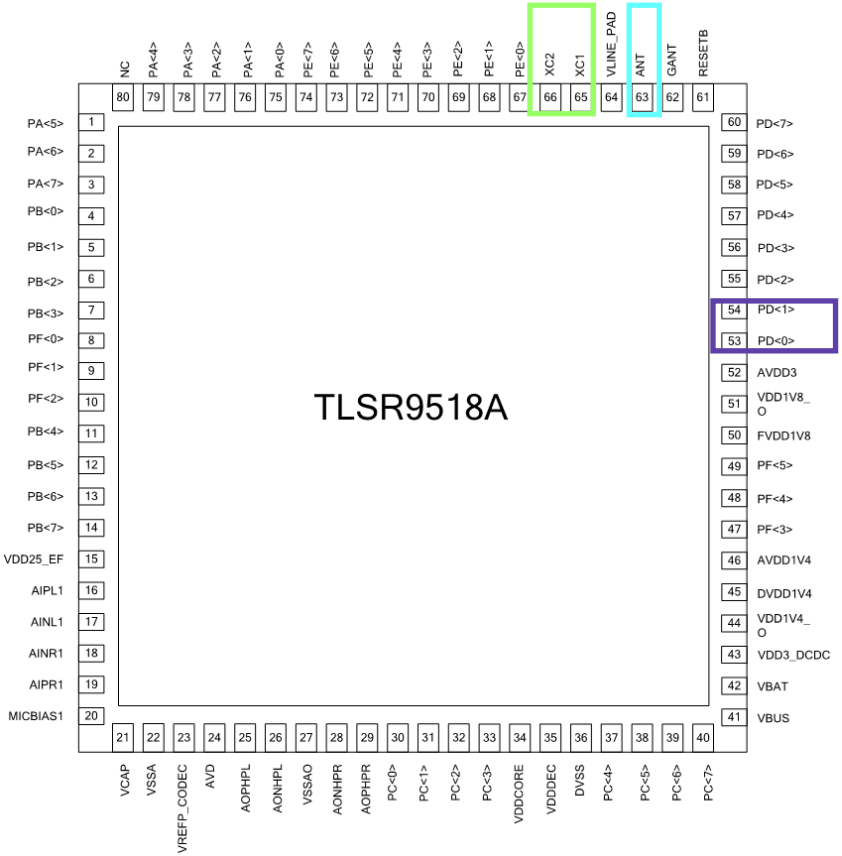
Note: If the customer is unable to determine whether the selected inductors meet the specification requirements, he/she can consult the Telink FAE and use the Telink development board to measure the efficiency. It is recommended to use a wire wound inductor with an efficiency greater than 80%.

Pin layout – Debug Port



- PIN3(PA7/SWS):
  - Download Pin and must be connected to a test point which is used to download FW.
- PIN1(PA5_DM)/PIN2(PA6_DP):
  - It is USB interface.
  - Recommend to connect to test points for capturing log when FW works.
- PIN71/PIN72/PIN73/PIN74:
  - A group of JTAG interface, and only supports 4-wire mode. Please refer to table 1-6 for detail.

Pin layout – RF Part: Part A

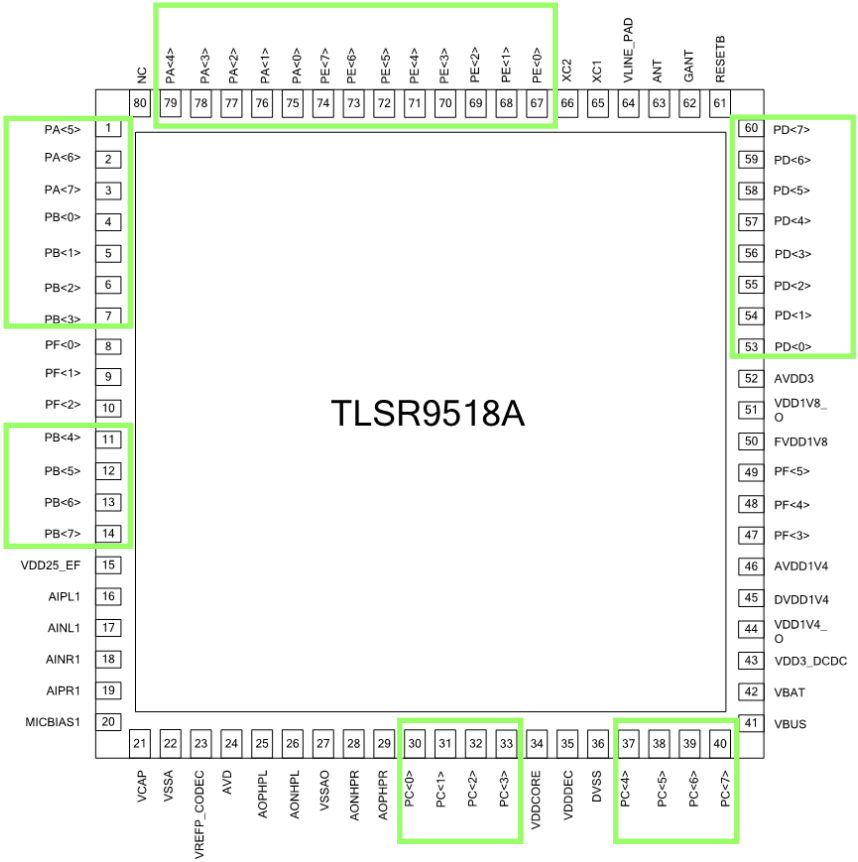


- RF Port:
  - PIN63(ANT) is RF port.
  - A 4th-order LC filter is recommend to use for certification. The detail will be introduced in the next page.
- 24Mhz Crystal:
  - PIN65(XC1), PIN66(XC2) connect 24Mhz crystal.
  - Usually recommended specification: 24Mhz – 12pF - +/-20ppm
    - Sometimes try different kind of 24Mhz crystal with different load capacitor, such as 10pf, 15pf because of different PCB layout to get lower frequency offset.
    - For some BLE projects, it is recommended to use the same type of crystal for TX/RX and to verify and calibrate the frequency bias according to different PCBs.
  - The range of internal load capacitor is among 5pF~18pF.
- 32.768K crystal:
  - PD0 and PD1 can be used to connect external 32.768Khz crystal.

Pin layout – RF Part: Part B

- A 4th-order LC filter is used for matching to pass certification, the values of which are flexibly adjustable corresponding to layout.
- Firstly, use VNA (Vector Network Analyzer) to do RX matching.
  - Customers must power on DUT, and use EMI tool to configure chip into RX mode, then tune RX matching.
- After RX test is finished, SA (Spectrum Analyzer) should be used to check TX harmonic.
  - If harmonics do not meet the requirements, re-do RX matching. Use the VNA to adjust component value to meet the impedance matching requirements, and then check TX harmonic again.
- It is recommend to mount a shielding box on PCBA for certification if customer can afford the cost. It is easy to pass certification and save time.
- TLSR9518A development board has passed FCC certification,
  - FCCID: OEOTLSR9518ADK80D

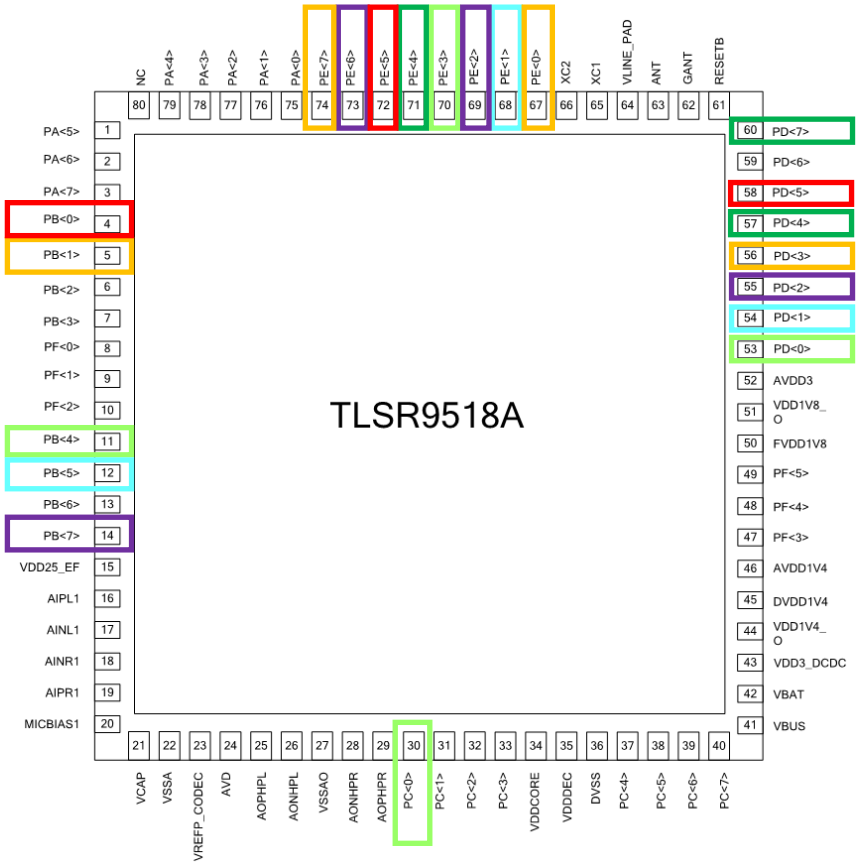
Pin layout – GPIO



- GPIO:
  - Refer to chapter 10.1.
  - All GPIO pins have configurable pull-up resistor and pull-down resistor.
    - Pull-up resistor: 10K/100K/1M
    - Pull-down resistor: 100K
  - Most of GPIO pins can be independently configured as high-level/low-level wakeup source, but some GPIOs can`t be used as wakeup source. Please refer to the description on datasheet.

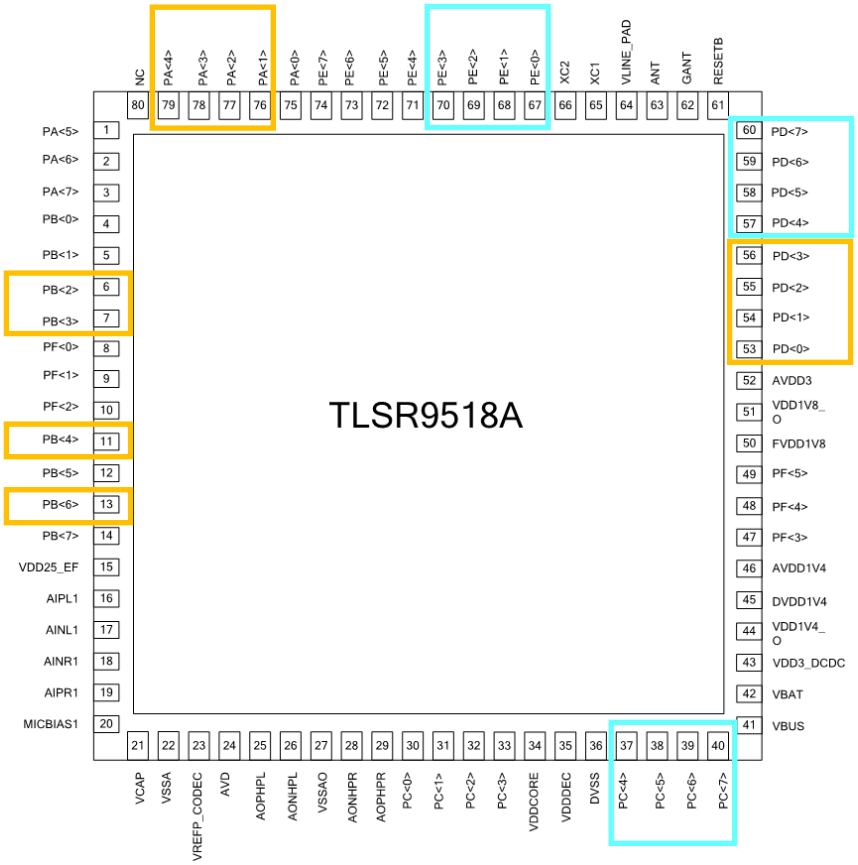
    NOTE:
    - *The default function of GPIO pins PE[5], PF[1] and PF[3] is outputting voltage, however, these pins cannot maintain high level or low level after deep sleep or deep retention sleep although they have pull-up/down resistor, therefore these pins are not suitable to be used for the applications that require stable voltage such as wakeup source.*
    - *The GPIO pins PF[0…5] for MSPI interface are not suitable to be used as wakeup source.*
  - Two kinds of driving strength:
    - PA[5:7],PE[0:1],PE[4:7]: maximum=8mA, minimum=4mA
    - Other GPIOs: maximum=4mA, minimum=2mA

Pin layout – PWM



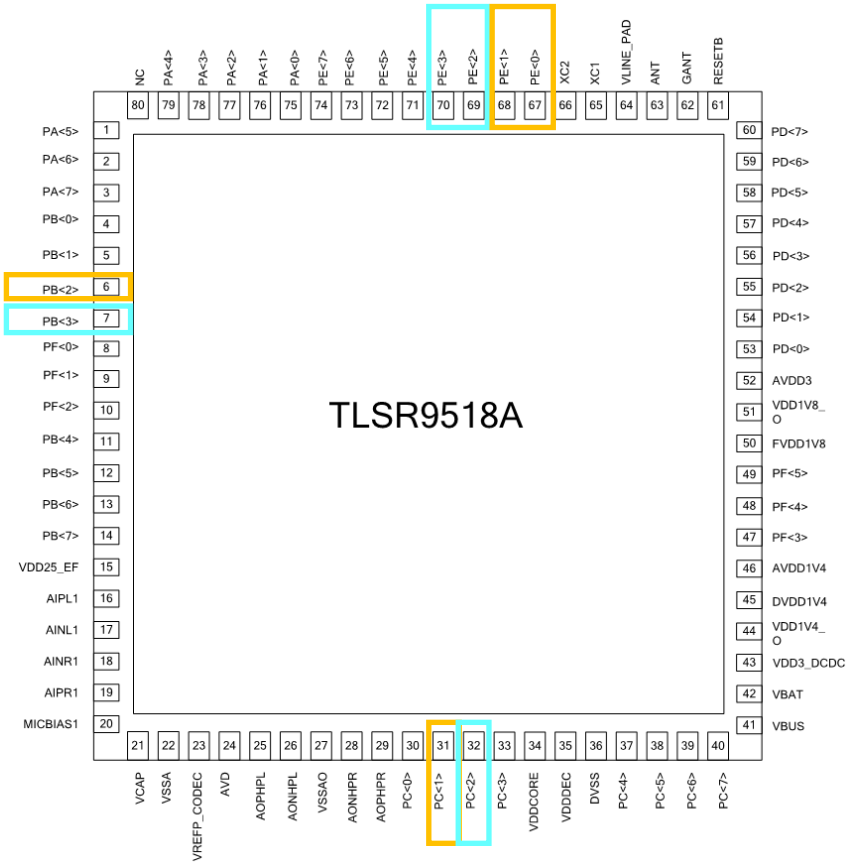
- PWM:
  - Up to 6 PWM output channels. Each PWMxn (x=0~5) has its corresponding inverted output pins, PWMxn_N pin.
  - PWM0 supports five modes, including Continuous mode (normal mode, default), Counting mode, IR mode, IR FIFO mode, IR DMA FIFO mode. PWM1~PWM5 only support Continuous mode.
    - PWM0: PB4/PC0/PE3
    - PWM0N: PD0
    - PWM1: PB5/PE1
    - PWM1N: PD1
    - PWM2: PB7/PE2
    - PWM2N: PD2/PE6
    - PWM3: PB1/PE0
    - PWM3N: PD3/PE7
    - PWM4: PD7/PE4
    - PWM4N: PD4
    - PWM5: PB0/PE5
    - PWM5N: PD5

Pin layout – UART



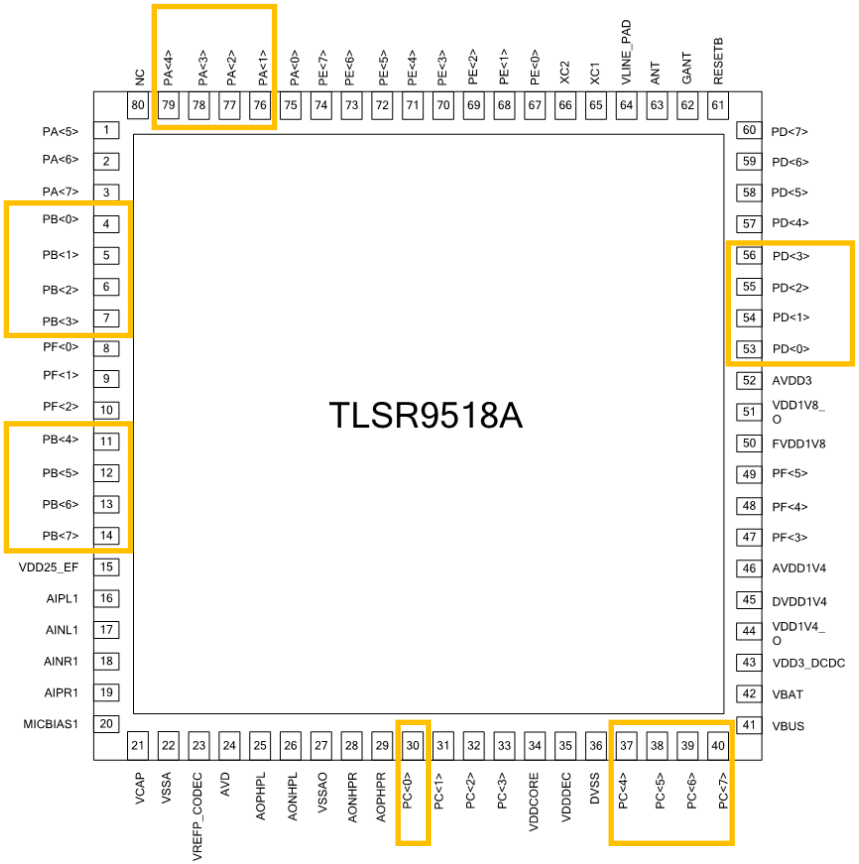
- Supports general UART interface and 7816 UART interface.
- Two groups of UART are supported, UART0 and UART1.
- UART0:
  - UTX: PA3/PB2/PD2
  - URX: PA4/PB3/PD3
  - CTS: PA1/PB6/PD0
  - RTS: PA2/PB4/PD1
- UART1:
  - UTX: PC6/PD6/PE0
  - URX: PC7/PD7/PE2
  - CTS: PC4/PD4/PE1
  - RTS: PC5/PD5/PE3
- If PDx/PCx port is used as UART, a capacitor (1nF) should be added to filter Spur.

Pin layout – I2C



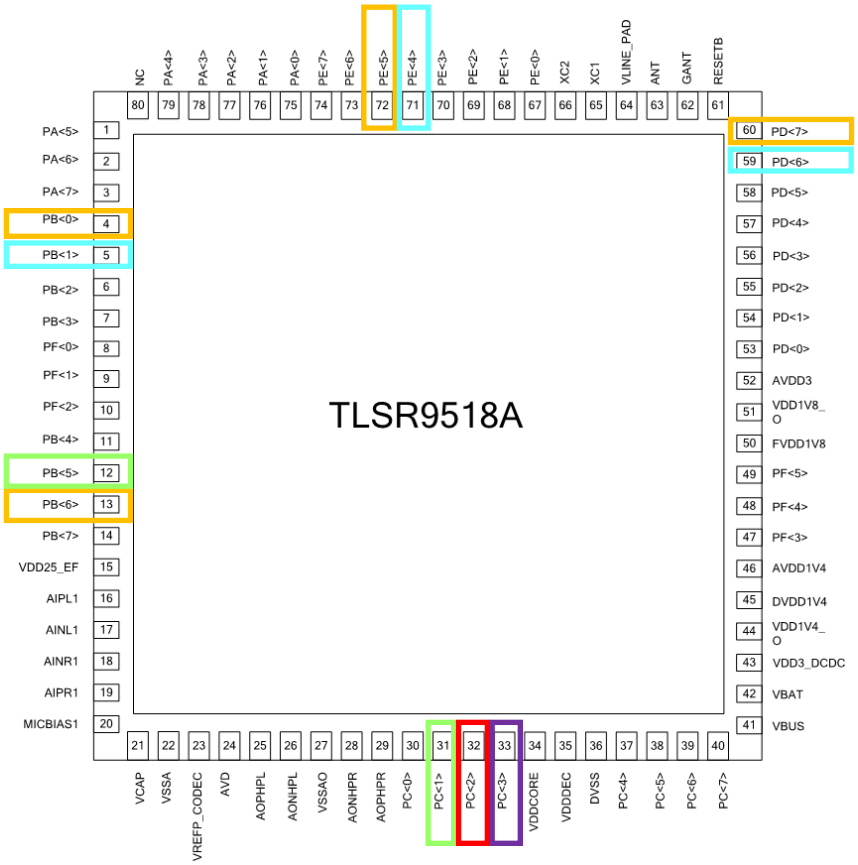
- The following IO ports can be configured as I2C interfaces
  - SCK: PB2/PC1/PE0/PE1
  - SDA: PB3/PC2/PE2/PE3
- Any SCK and SDA can be used in combination
- Support master and slave mode
- For supporting up to 400K bit/s, external pull-up resistors must be added.

Pin layout – SPI



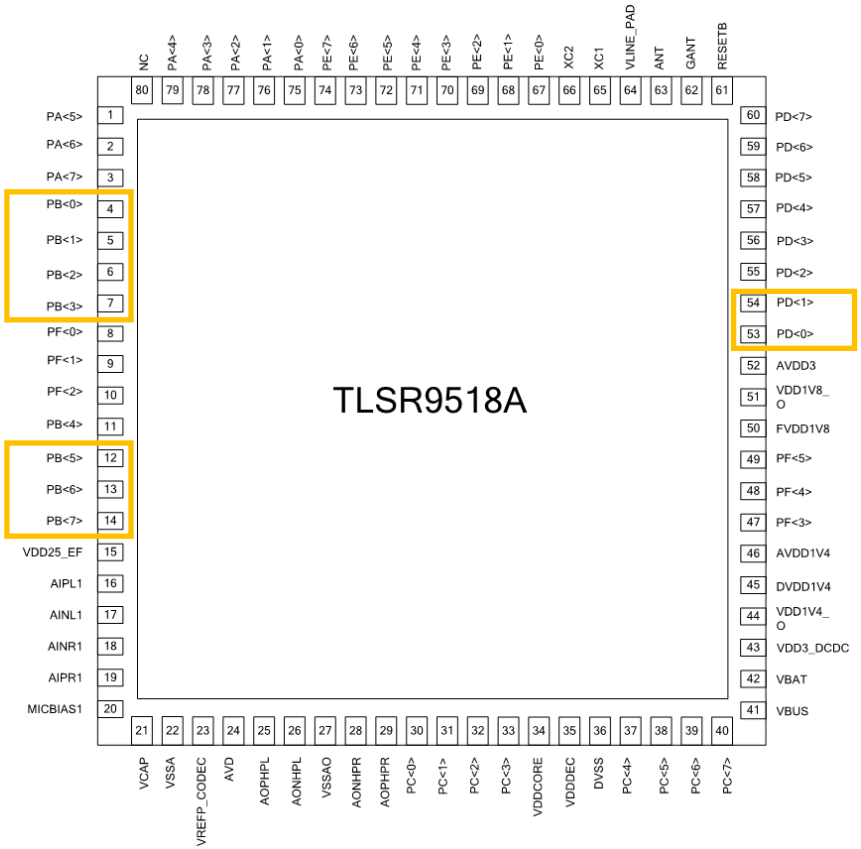
- Supports memory SPI, HSPI, PSPI and SPI_SLV.
- SPI_SLV interface:
  - CLK/CSN/MOSI/MISO: PA2 / PA1 / PA3 / PA4
- SPI - HSPI:
  - Supports master/slave mode, used in high performance application.
    - CLK: PB4 / PA2
    - CSN: PB6 / PA1
    - MOSI_IO0: PB3 / PA4
    - MISO_IO1: PB2 / PA3
    - WP_IO2: PB1
    - HOLD_IO3: PB0
- SPI - PSPI:
  - Supports master/slave mode, used in low power application.
    - CLK: PC5 / PB5 / PD1
    - CSN: PC4 / PC0 / PD0
    - MOSI_IO0: PC7 / PB7 / PD3
    - MISO_IO1: PC6 / PB6 / PD2

Pin layout – RF front-end & Antenna Select Pins



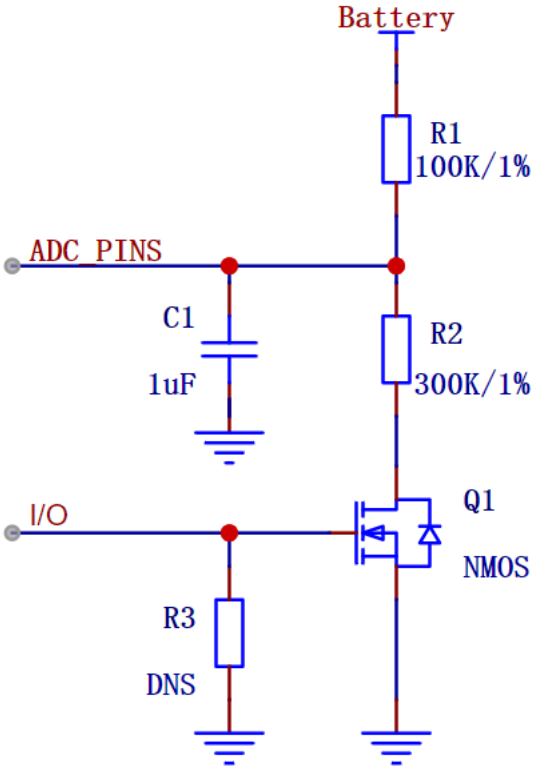
- External RF front-end Pins:
  - TXCYC is used to control the PA (Power Amplifier) of external RF Front-end: PB0 / PB6 / PD7 / PE5.
  - RXCYC is used to control the LNA of external RF Front-end: PB1 / PD6 / PE4.
- Antenna Select Pins:
  - One groups of SEL<0:2> are used to select one of up to eight external antennas. The selected antenna channel is connected to the RF_IO pin.
    - ATSEL0 - PB5/PC1
    - ATSEL1 - PC2
    - ATSEL2 - PC3

Pin layout – ADC Pins: Part A



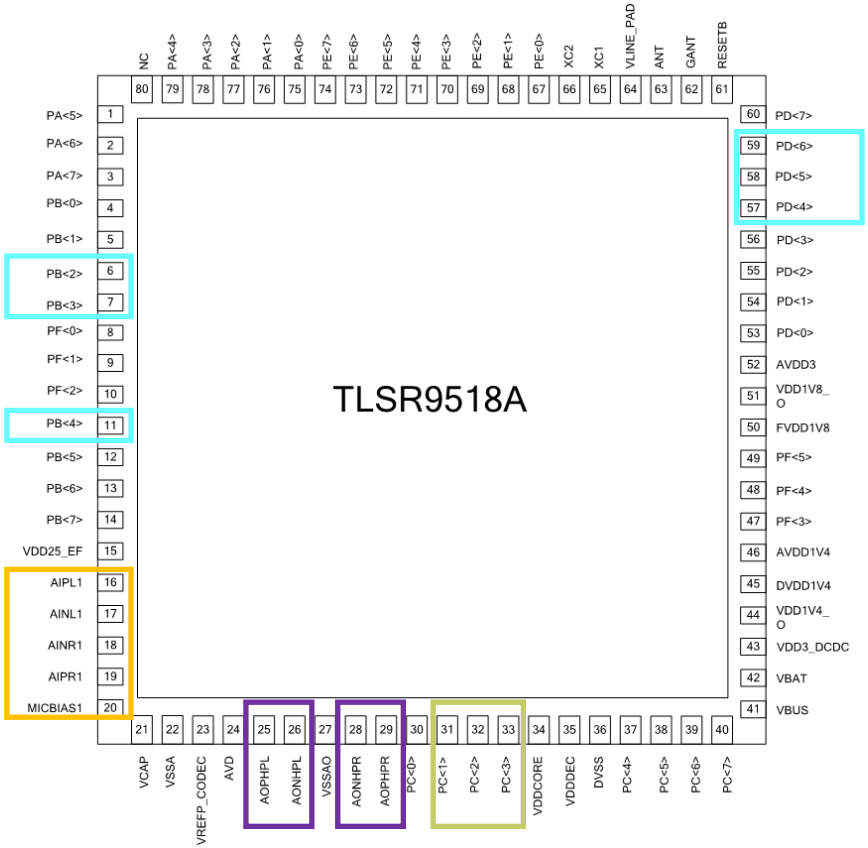
- ADC:
  - Supports up to 10 detect pins, including PB0~PB7, PD0~PD1.
- Battery voltage detection:
  - For applications where the power supply is below 3.6V, the battery can be connected directly to the VBAT pin, but this method has a lower detection accuracy. Recommended ADC for battery voltage detection
  - For applications where the power supply is above 3.6V, the battery can only be connected to an ADC detection pin for voltage detection through a voltage divider resistor.
  - If the system is powered by only one AAA batteries, it needs to be connected to a boosted DCDC. Then use Vbat direct detection or ADC detection for voltage detection

Pin layout – ADC Pins: Part B



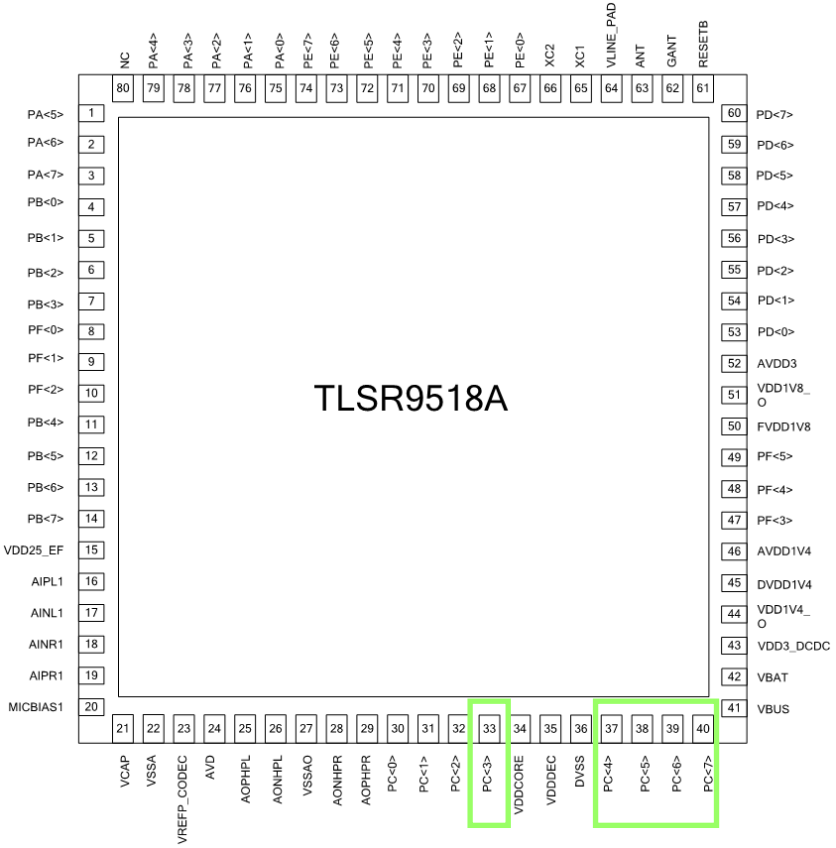
- Recommended Battery Voltage Detection Reference Circuits for Audio Application Solutions
  - Considering that the battery voltage is up to 4.2V when powered by the li-ion battery, a voltage divider circuit is needed.In addition, to ensure low static power consumption, the voltage divider circuit needs to be turned off when voltage detection is not required. Therefore an additional switching circuit is required

Pin layout – Audio Part: Part A



- Audio input path - AMIC:
  - Supports 2 channels, including both differential and single mode.
  - PIN16(AIPL1)/PIN17(AINL1) are channel 1, higher priority.
  - PIN18(AINR1)/PIN19(AIPR1) are channel 2.
  - PIN20 (MICBIAS1) is the microphone power supply pin.
- Audio input path – DMIC:
  - Two groups of PINs can be configured as DMIC signal.
    - PB2/3/4 – Data/Clk0/Clk1
    - PC1/2/3 - Data/Clk0/Clk1
    - PD4/5/6 - Data/Clk0/Clk1
- Audio output path:
  - Supports 2 channels, only differential mode.
  - PIN25(AOPHPL)/PIN26(AONHPL) are L channel.
  - PIN28(AONHPR)/PIN29(AOPHPR) are R channel.

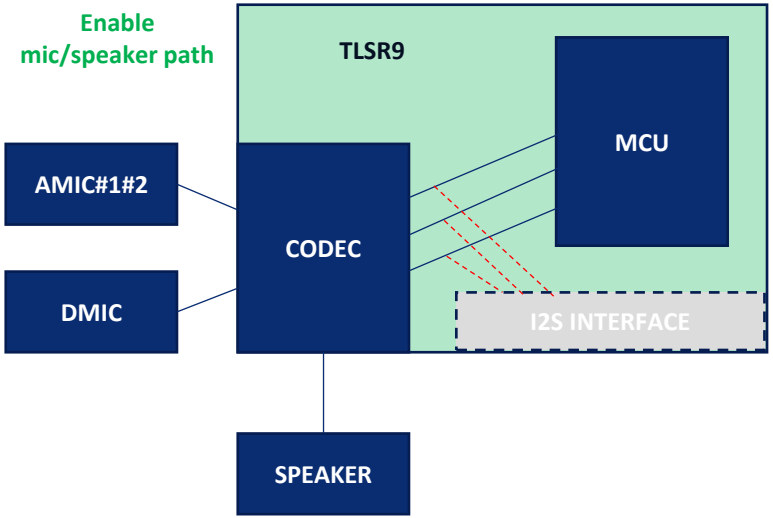
Pin layout – Audio Part: Part B

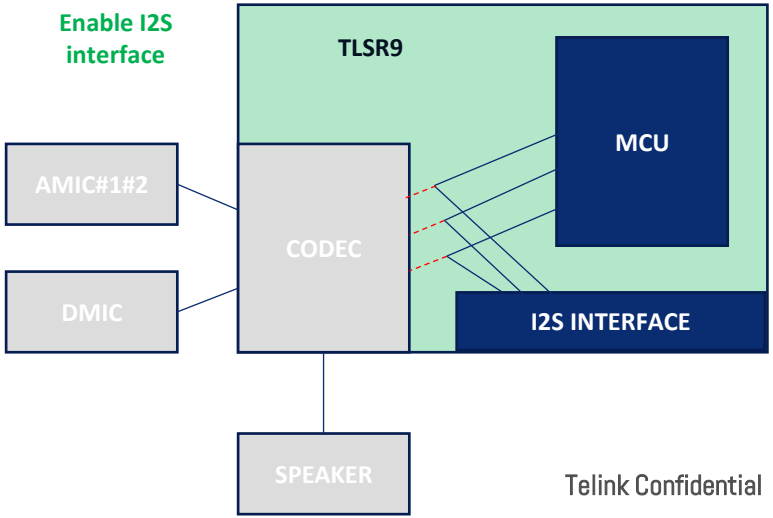


- I2S interface:
  - Supports one group I2S pins
  - When working in 5-wires mode,
    - PC3 - bit clk
    - PC4 - output frame clk
    - PC5 - output data
    - PC6 - input frame clk
    - PC7 - input data
  - When working in 4-wires mode,
    - PC3 - bit clk
    - PC4 - output frame clk
    - PC5 - output data
    - PC7 - input data

Pin layout – Codec Part: Part A

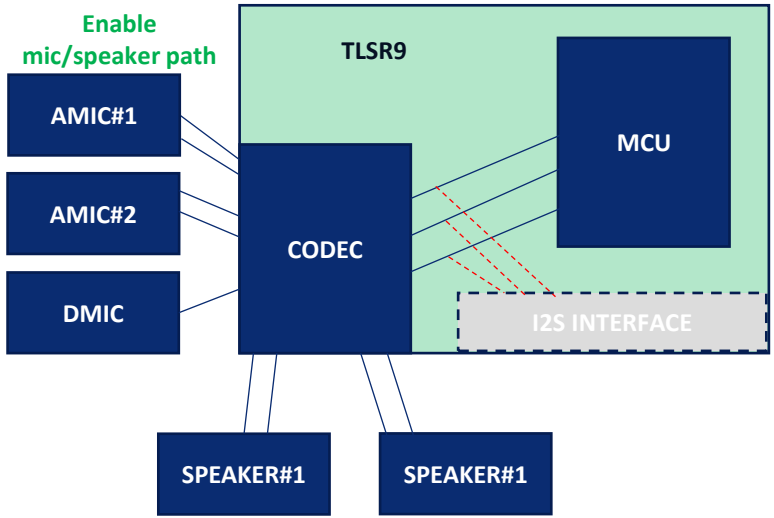
- Internal codec and I2S interface can`t work together because the I2S interface is shared.
  - When AMIC/DMIC or output audio path are enabled, I2S interface can’t be used to communicate with the external codec.
  - When using I2S interface to communicate with an external codec, AMIC/DMIC or output audio path won’t work.





Pin layout – Codec Part: Part B

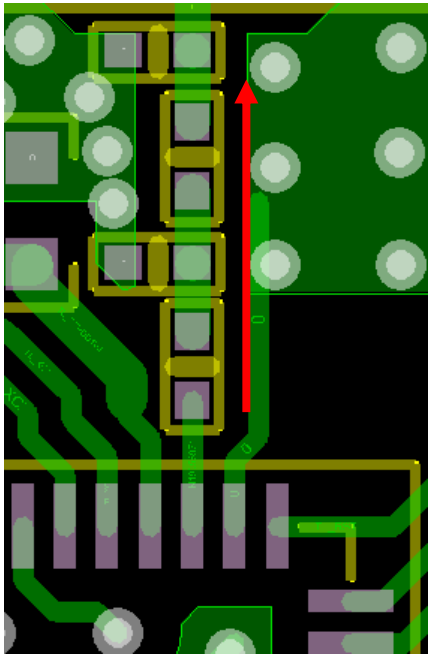
- When internal codec is enabled, TLSR9 can support dual analog input channels - both differential and single-ended mode.
- When internal codec is enabled, TLSR9 codec supports dual analog output in differential mode only, no single-ended mode. The load should be either 16 or 32 Ohms.

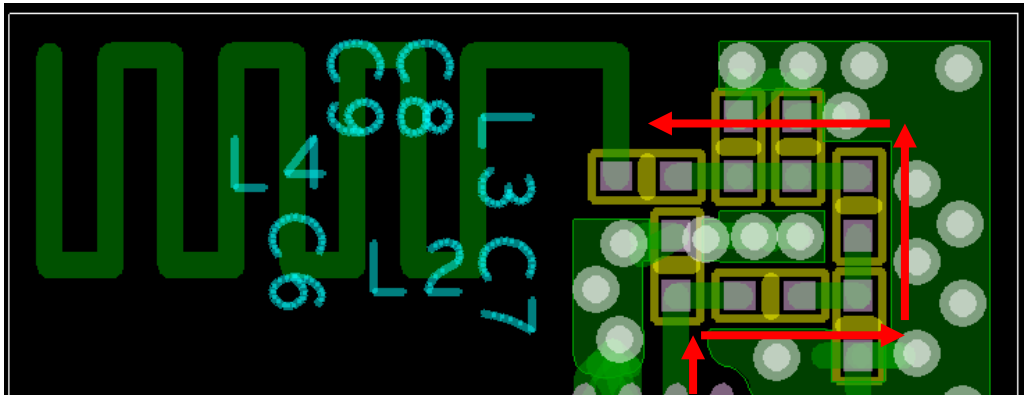


PCB Design Guideline

RF layout

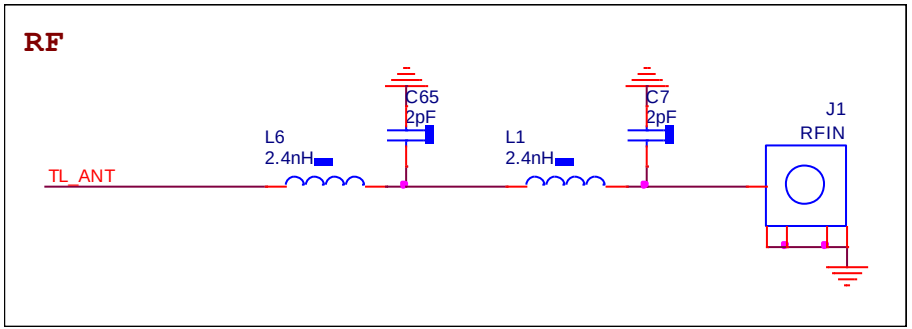
- The components on the RF path MUST be placed one by one. and they MUST be placed close to each other, no stub.
- It the area is not enough, can fold it, but MUST use ground and via to shield RF trace.

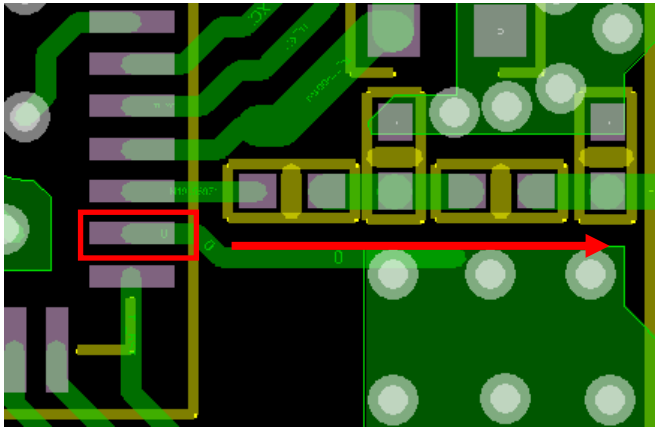




GANT PAD

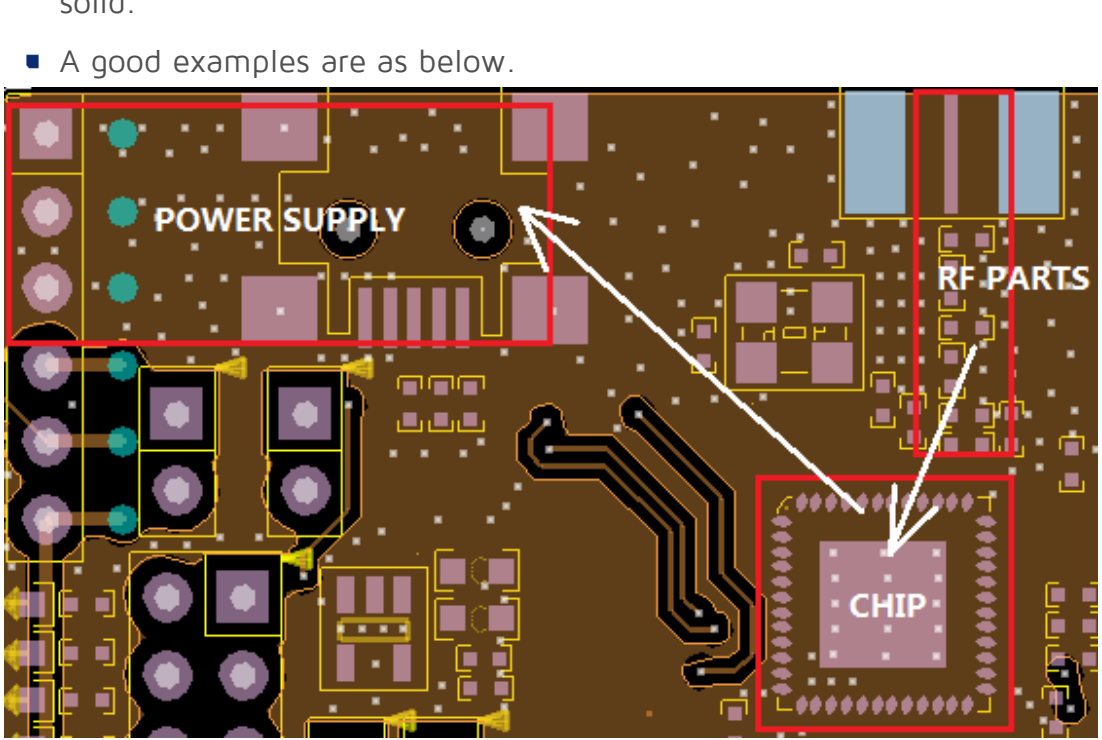
- GANT pad, which is in the red box, MUST be connected out. And CAN`T connect it to E-PAD directly.
- Recommend to use 4th-order filter to pass certification.

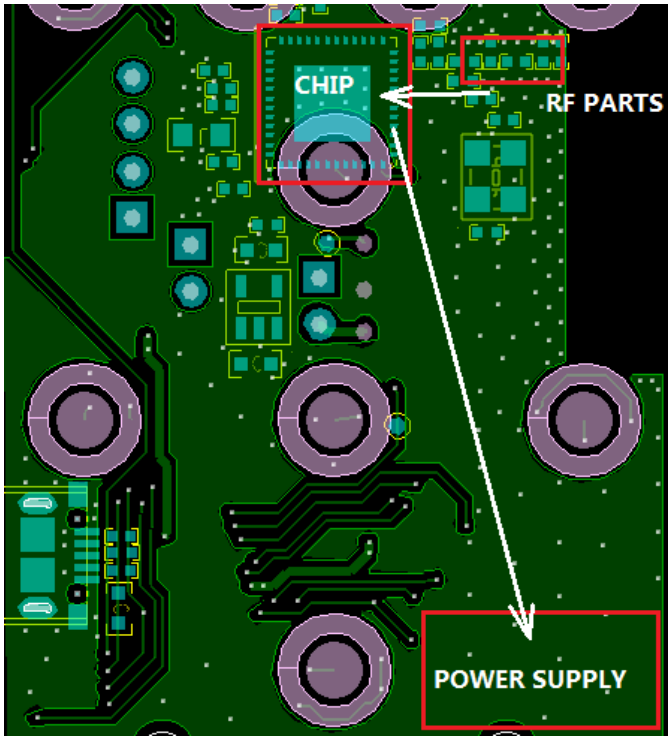




Solid Ground Plane

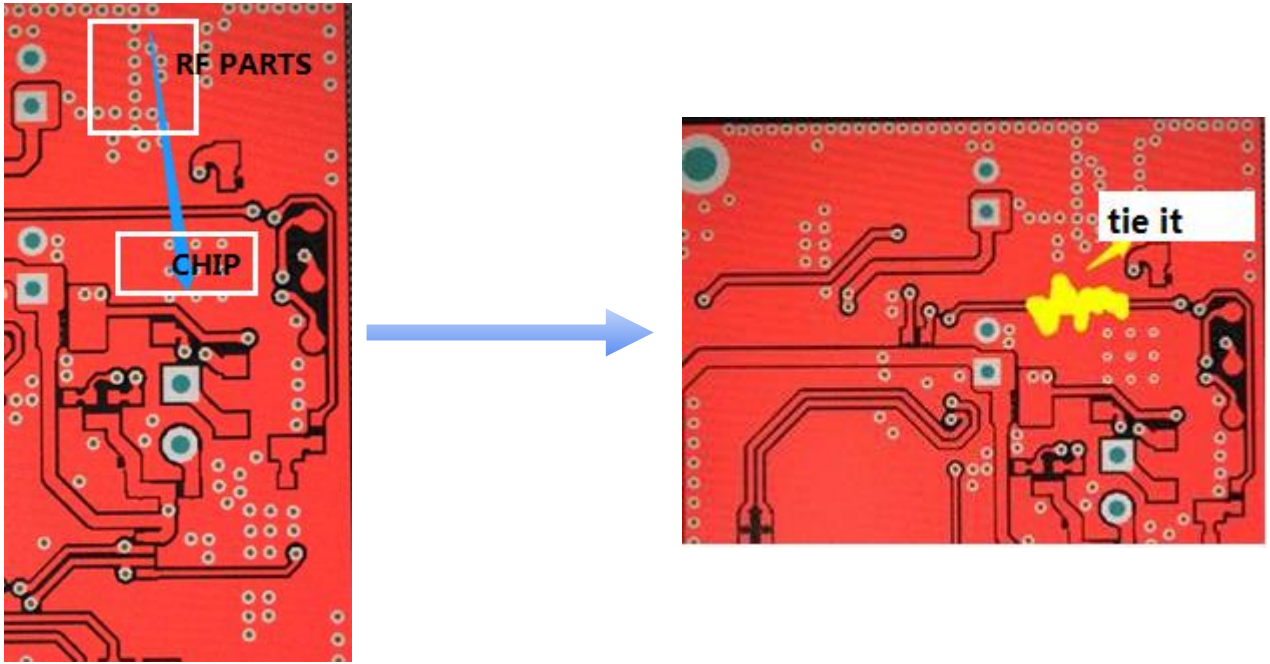
- The ground plane MUST be wide, solid. The ground plane from power supply to chip, then at last to RF parts MUST be solid.
- A good examples are as below.





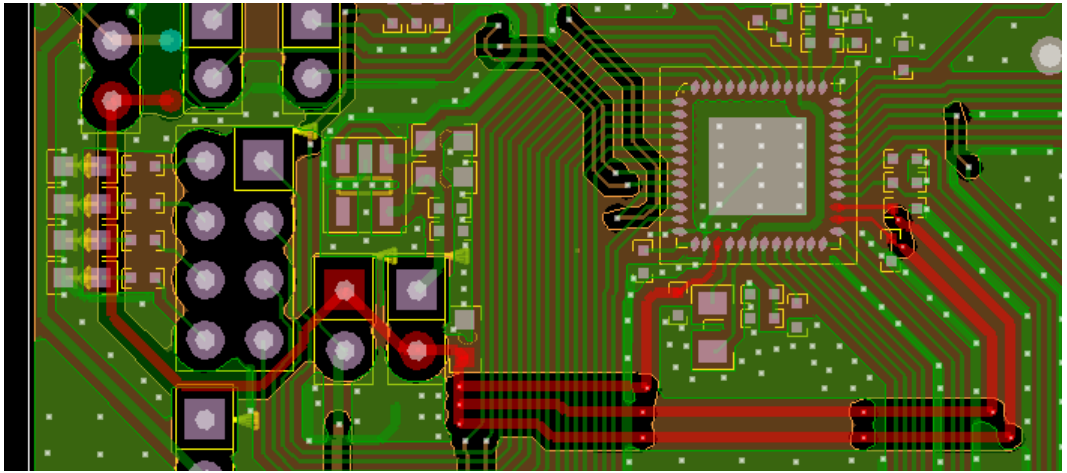
Solid Ground Plane(Cont)

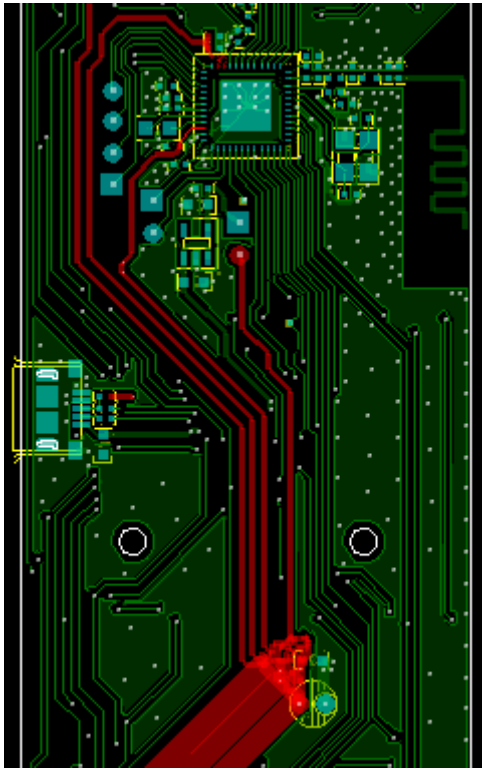
- A bad example is as below.
  - Ground plane between RF parts and chip is cut off, the rx performance is greatly affected.
  - Tie them together, the RX performance matches the data on the datasheet.



Star connection

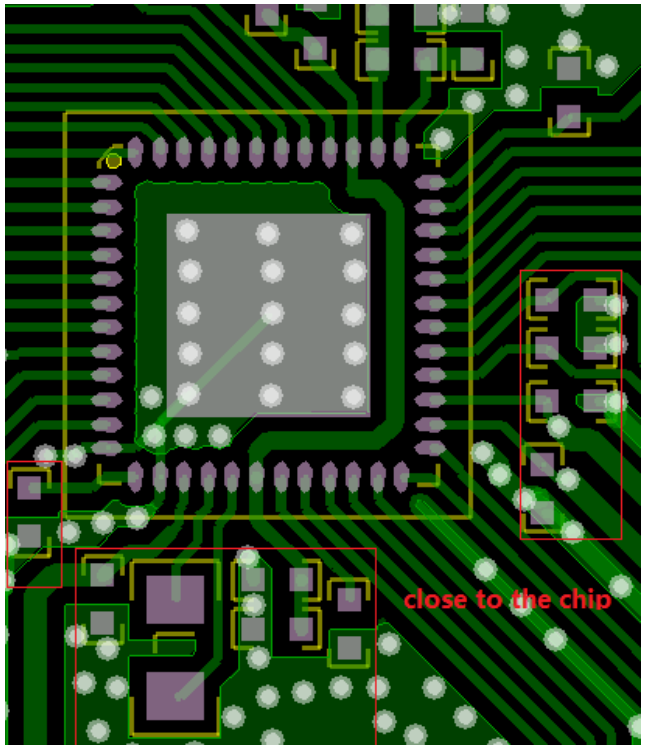
- Power supply should be connected in star-type connection.
  - If there is no audio function, can connect them together.

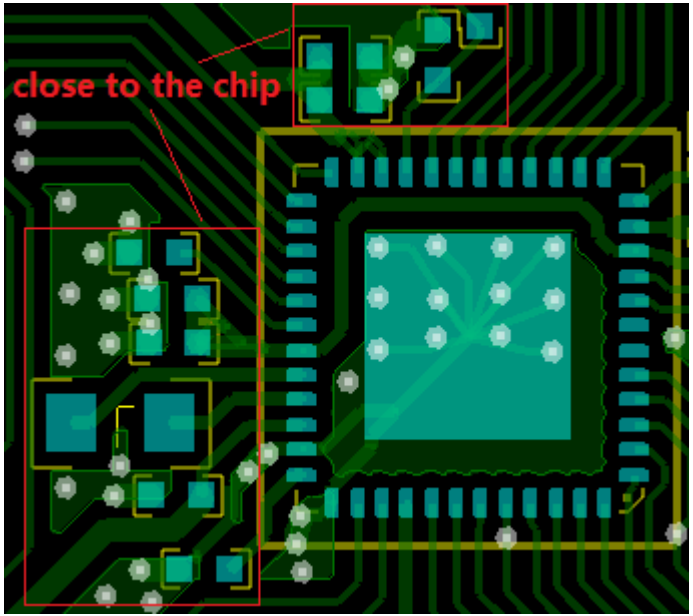




Decoupling capacitor

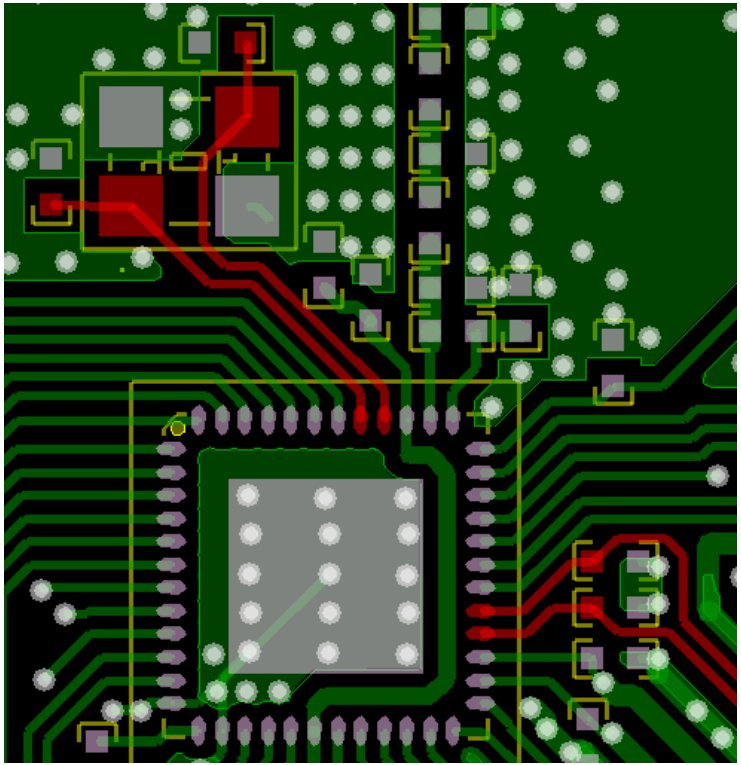
- Decoupling capacitors MUST be placed close to power pins.

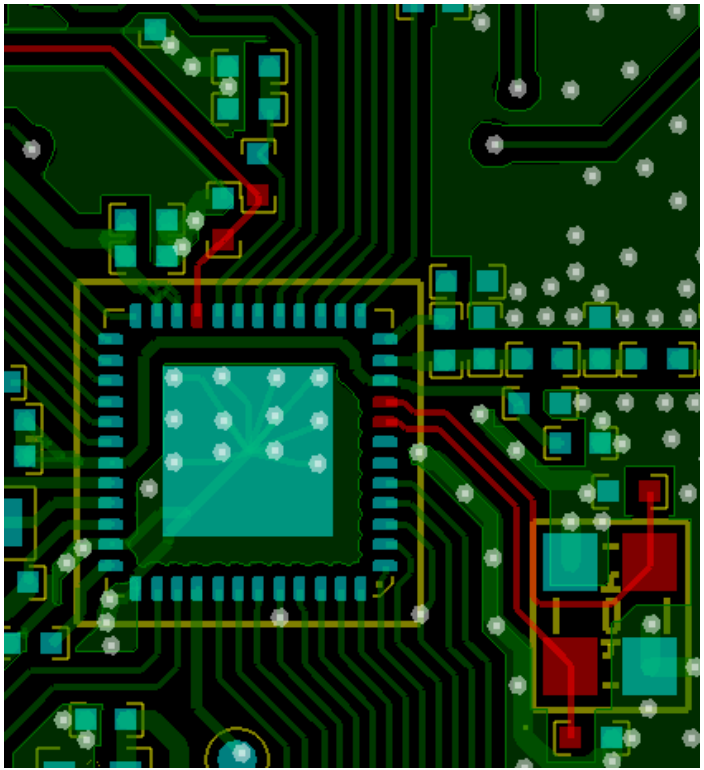




Key traces

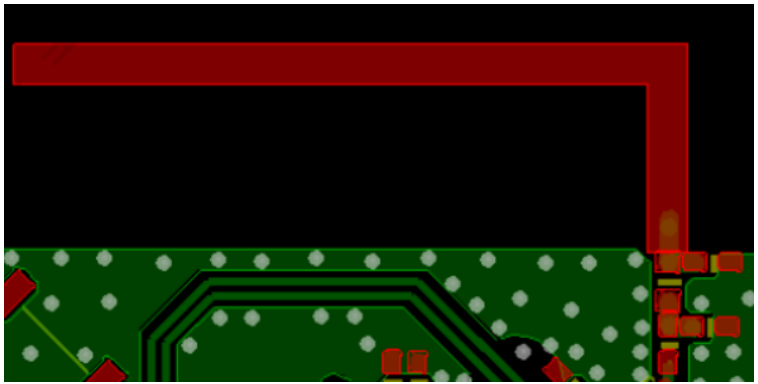
- To avoid EMI issue, some important parts such as crystal, audio trace, mic trace and usb trace MUST be shielded by GND and via.





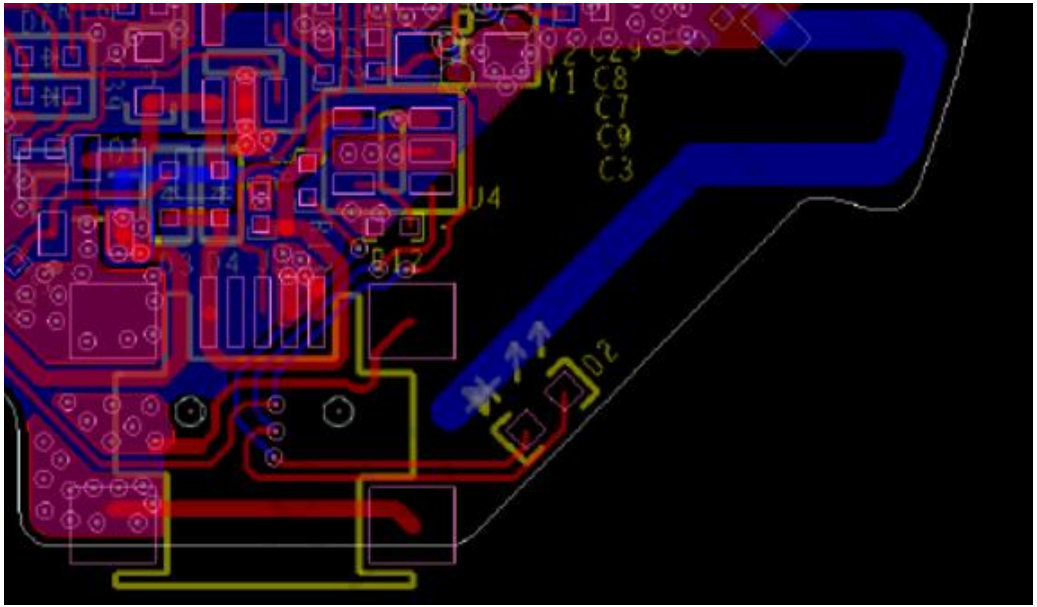
Antenna – common requirement

- Antenna trace width shouldn`t be too narrow in order to decrease loss.
- Line width should be 0.5mm or above, generally it`s recommended to be 0.5mm or 1mm.
- Top and bottom of antenna location should not be covered by GND.
- The distance between antenna and GND should be 3mm or above.
- Generally antenna length is 20mm~30mm. The smaller the GND is, the longer the antenna should be.



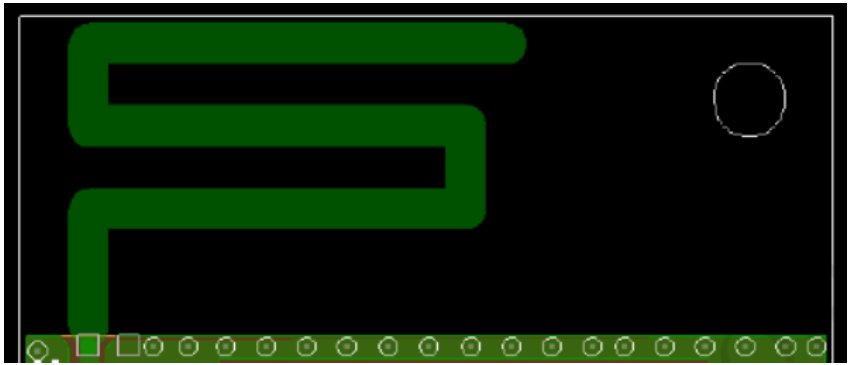
Antenna – keep away others

- Keep PCB antenna far away from metal, battery, or other components, such as 3mm or 5mm.
- A bad example is showed as below. The antenna is too close to USB connector.



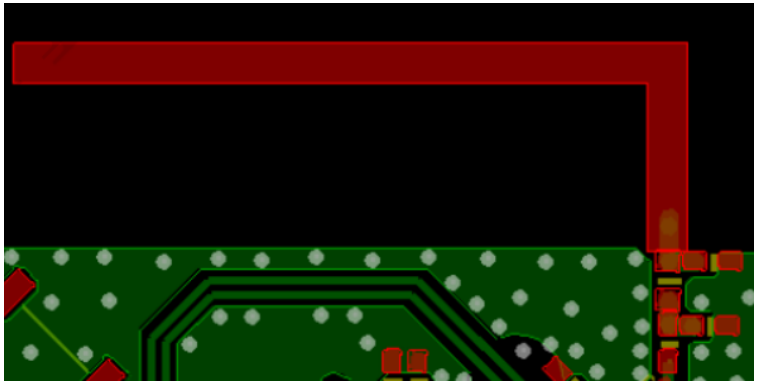
Antenna – don`t exposed to others

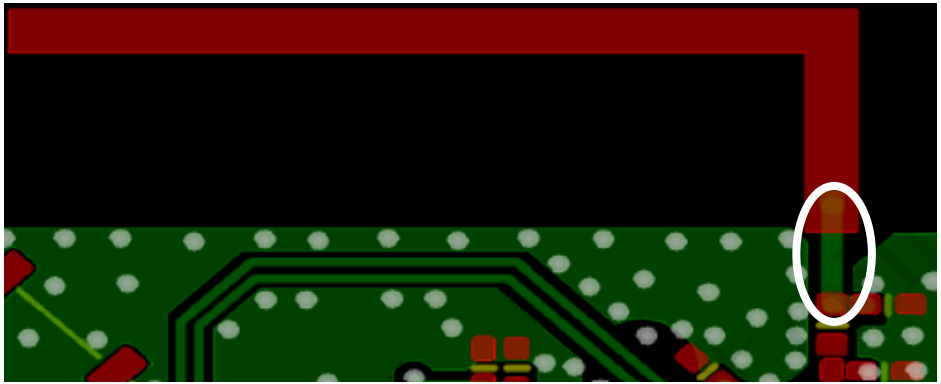
- There MUST be a row of via holes along the antenna on the side parallel to GND. Do not directly expose trace or pad to the antenna.
- The left is a good example. The right is a bad example.



Antenna – matching components

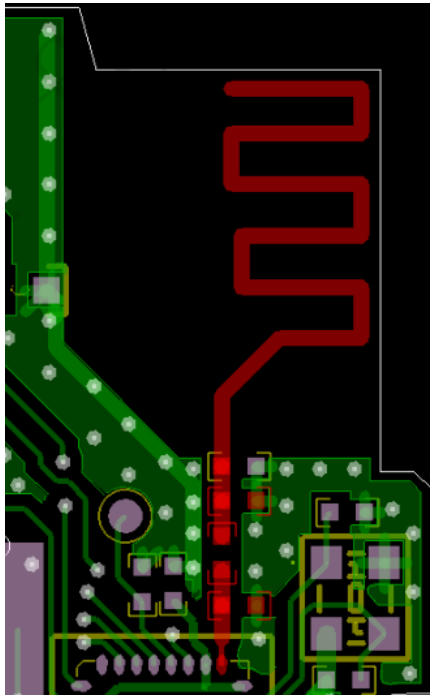
- Antenna matching components should be placed at the boundary of antenna and GND without shrink inward or expand outward.
- The left is a good example. The right is a bad example.

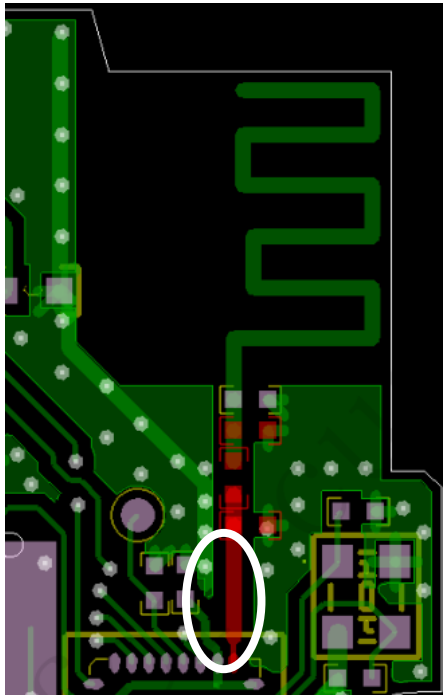




Antenna – impedance design

- The RF line to the antenna port should be short. If RF trace can`t be designed shortly, it must be designed as 50ohm micro-strip line.
- The left is a good example. The right is a bad example.

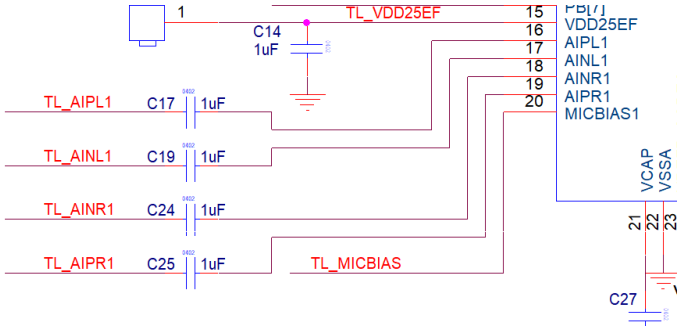


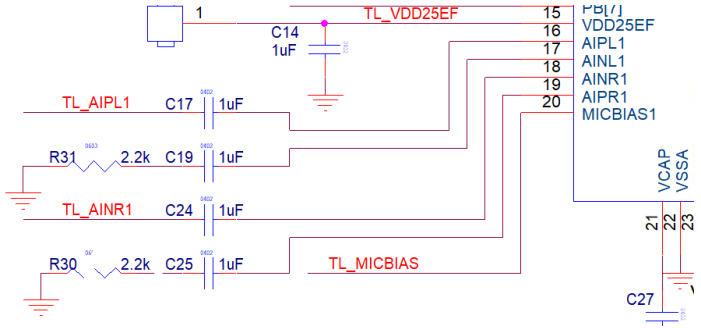


Audio Design Guideline

Audio Input – Codec

- Support two audio input channels, MIC_L has a higher priority.
- Supports both differential and single-ended inputs:
  - Differential Inputs.
    - AIP/AIN are connected in series with 1uF capacitor respectively.
  - Single-ended input.
    - AIP series connected 1uF capacitor. AIN series resistor and capacitor to ground.
    - The software is configured according to the differential connection method.
    - If the chip is reserve only one AIP, the software uses a single-ended configuration.

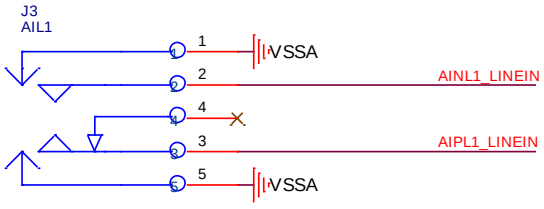




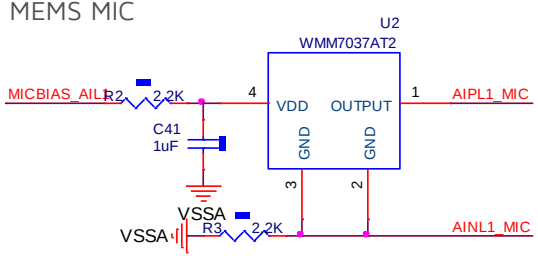
Audio Input – Codec AMIC

- LINE IN:
  - This method can be connected to a differential input 3.5 mm audio jack.
- MEMS MIC:
  - Both the positive and negative terminals of MIC need to be connected.
  - MICBIAS needs attention to add filtering.

LINE IN



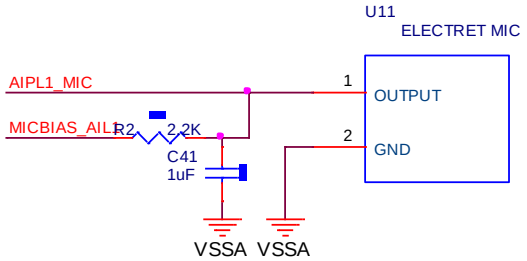
MEMS MIC



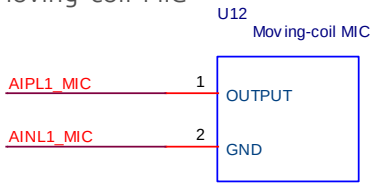
Audio Input – Codec AMIC

- ELECTRET MIC:
  - MICBIAS needs attention to add filtering.
  - Chip's AIN needs to be connected to resistor to ground.
- Moving-coil MIC:
  - According to the differential connection method.

ELECTRET MIC

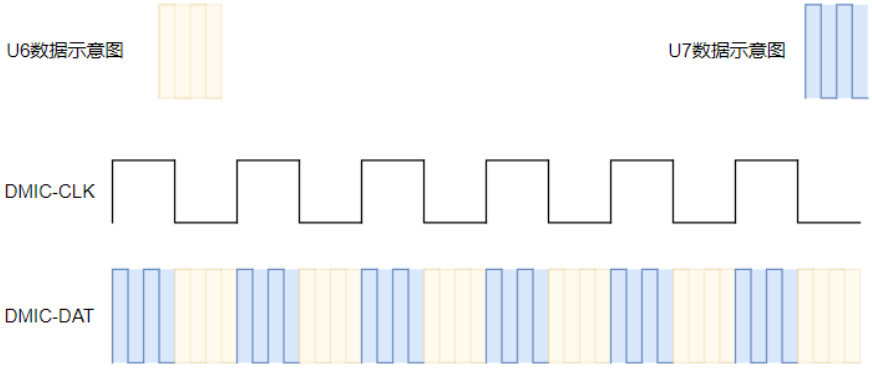


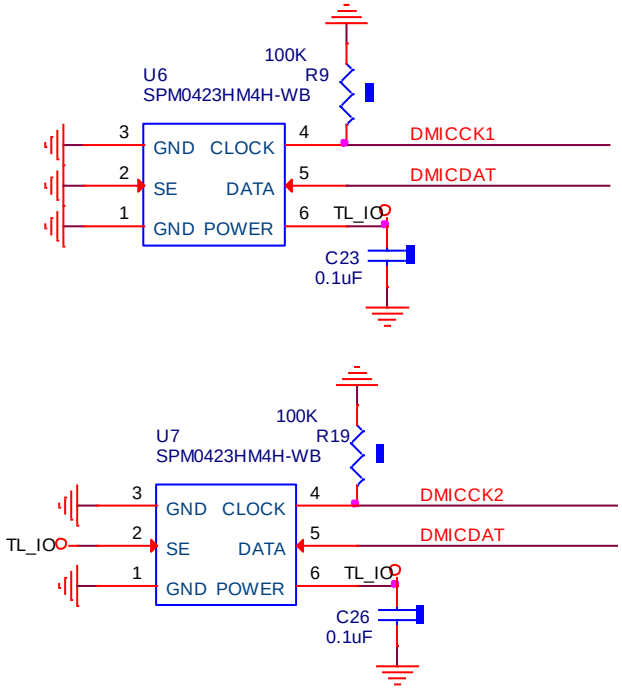
Moving-coil MIC



Audio Input – Codec DMIC

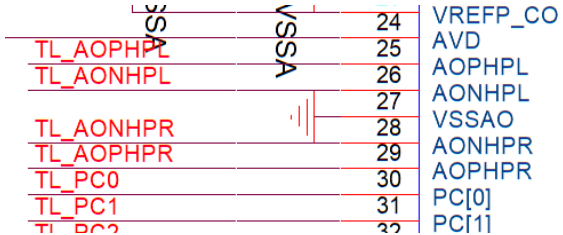
- Audio input path – DMIC:
  - Supports two digital microphone inputs.

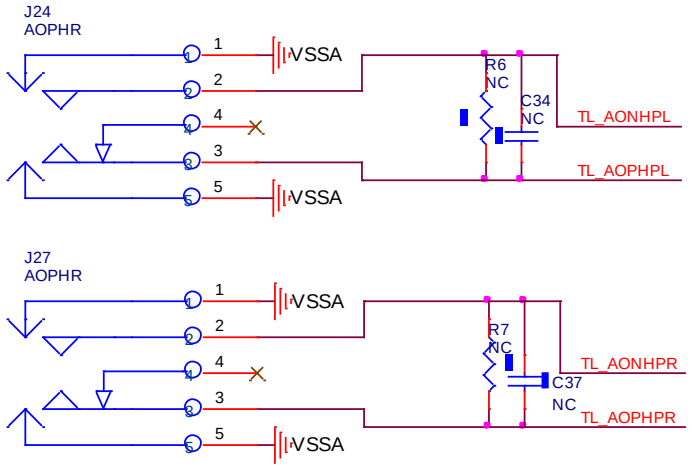




Audio Output – Codec

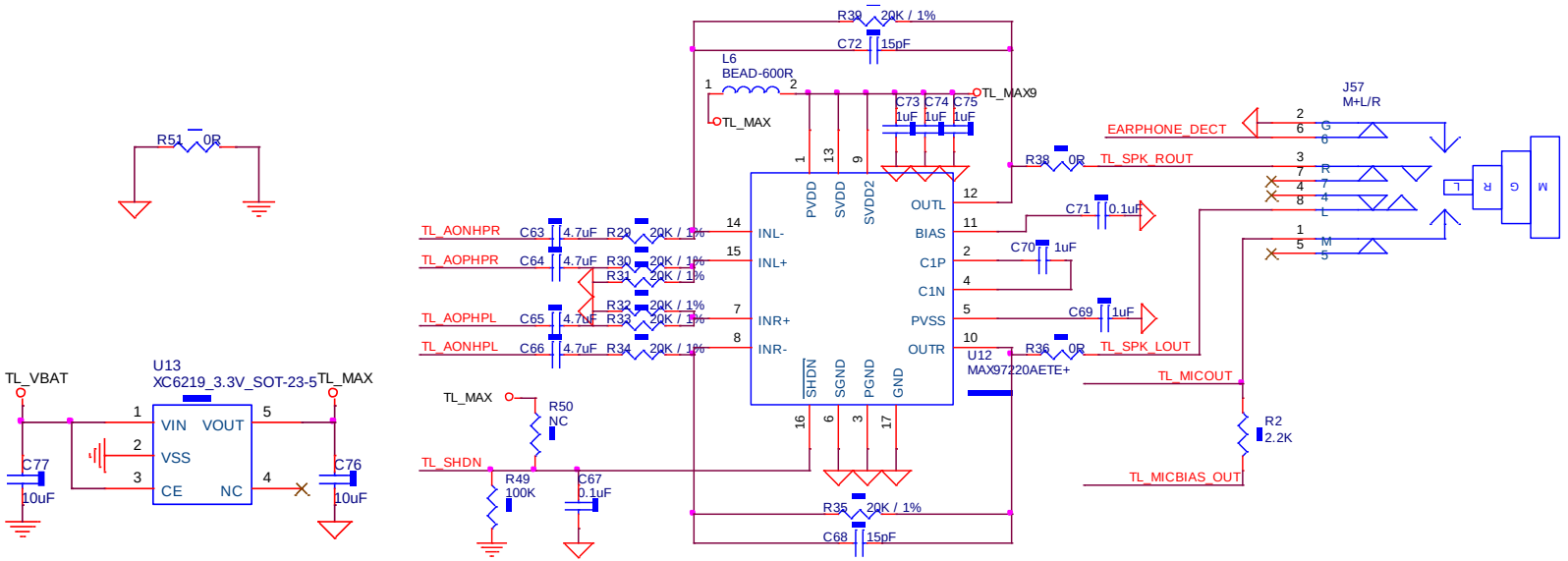
- Audio support stereo channel output, only support differential connection
  - AOPHPL and AONHPL are the positive and negative poles of the audio left channel output.
  - AOPHPR and AONHPR are the positive and negative poles of the audio right channel output.
  - The left and right channels are connected to the speakers, supporting 16ohm and 32ohm load.





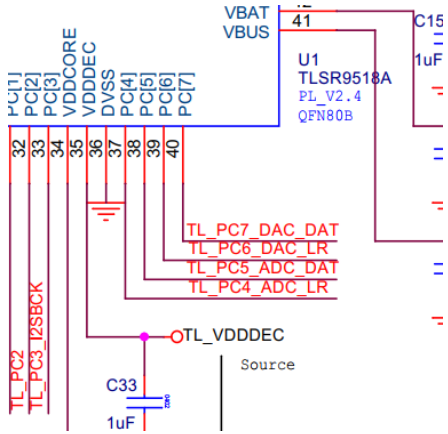
Audio Output – Codec

- Single-ended audio output, requires additional differential to single-ended chip
- Differential to single-ended part of the analog ground and chip ground with 0R resistor for isolation.
- A LDO is set separately for the power supply of the differential to single-ended part, isolating the power supply from the chip power supply.



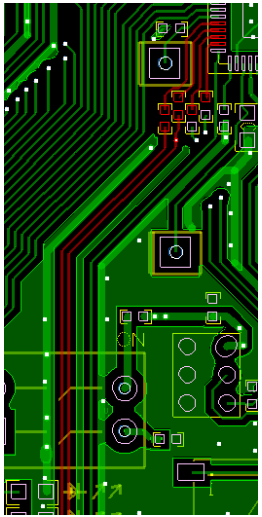
Audio Input/Output I2S

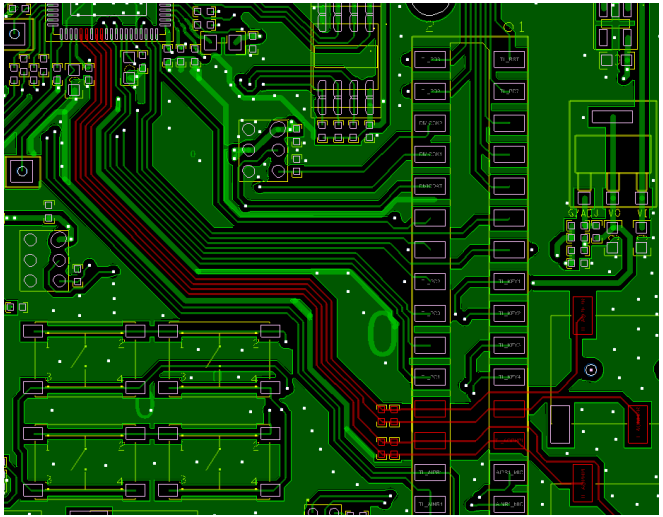
- I2S interface:
  - 5-wires mode
    - PC3/PC4/PC5/PC6/PC7 - BCLK / OUTPUT_LRCLK / OUTPUT DATA / INPUT LRCLK / INPUT DATA
  - 4-wires mode, Not connected to PC6, Input and output clocks ensure consistency.
    - PC3/PC4/PC5/PC7 - BCLK / OUTPUT_LRCLK / OUTPUT DATA / INPUT DATA
- I2S and Codec cannot be used for audio input or output at the same time, see Page21/22 for details.



Audio – Layout Design

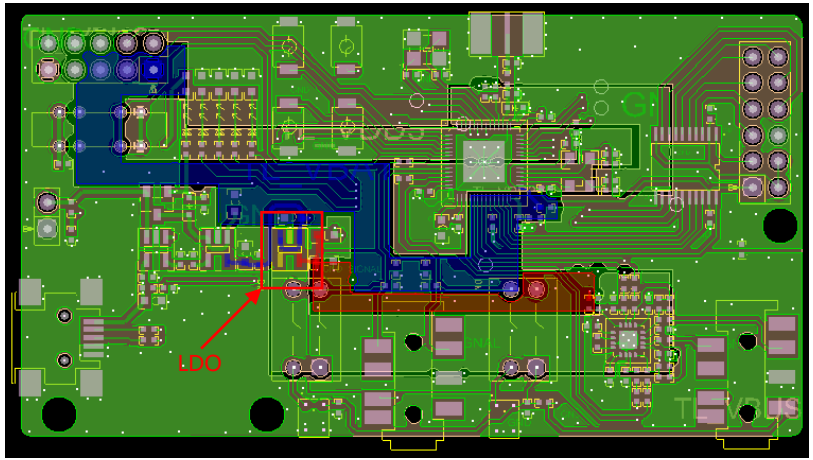
- Audio Input&Output:
  - Audio routing can't be parallel to the power line and high-speed signal lines, and as far away as possible, pay attention to crossover routing.
  - Audio alignment try not to change the layer over the hole.
  - Attention to the ground package treatment.

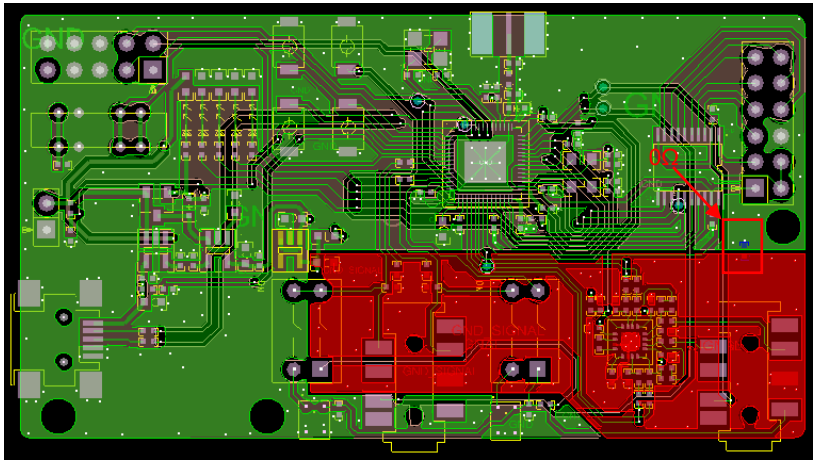




Audio – Layout Design

- Differential to single-ended chip section
  - The power supply of this part needs to be isolated from the power supply of the chip through the LDO.
  - The analog ground of this part needs to be isolated from the chip part ground by a 0Ω resistor.





Change Logs

- 2021.01.05:
  - Initial version
- 2021.02.01:
  - Update Pin description.
- 2022.02.12:
  - Rewrite the section about pin layout.
- 2022.03.16:
  - Update Pin description.
- 2022.03.24:
  - Add Audio section reference design.
- 2023.10.23:
  - Add DCDC inductor requirment and battery voltage detection reference circuits
- 2023.12.08:
  - Update GPIOs part which can`t be used as wakeup source.