Telink

Telink Semiconductor

B92 Hardware Design Guideline

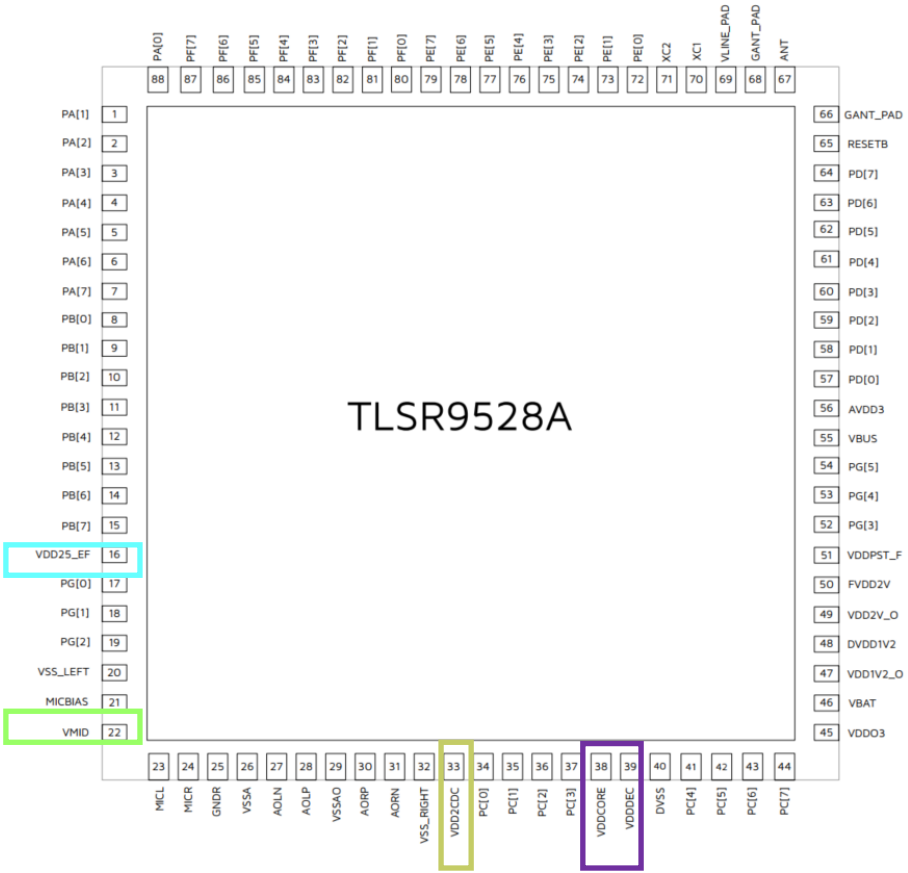
2023-3

Scope

- Chip`s datasheet is the basic reference file of hardware design. This document will go through datasheet with hardware engineer and supplement some details. It will speed up projects after reading the document.
- Considering that the chip`s datasheet will be continuously updated, if there is any difference between this document and the chip`s datasheet, please refer to the latest version of the chip specifications.
- The version and link of the chip`s datasheet mentioned in this document are as follows:
  - TBD
    - http://wiki.telink-semi.cn/wiki/chip-series/TLSR9-Series/
- TLSR9528A is taken as an example to describe. And the content mentioned in the file applies to the B92 chipset serials.

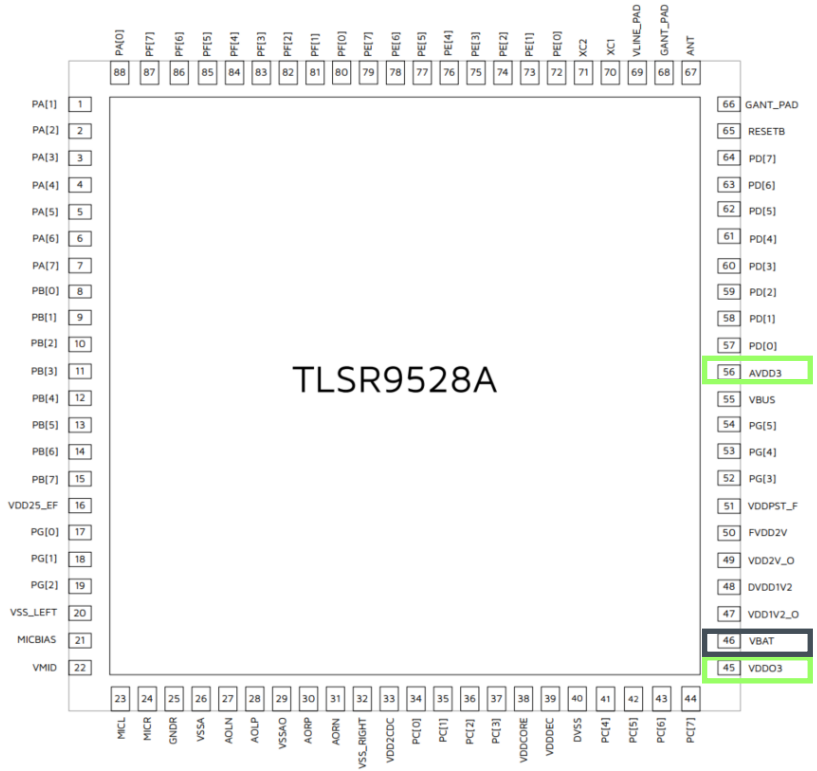
Schematic Design Guideline

Pin layout – Power Supplies : Part A



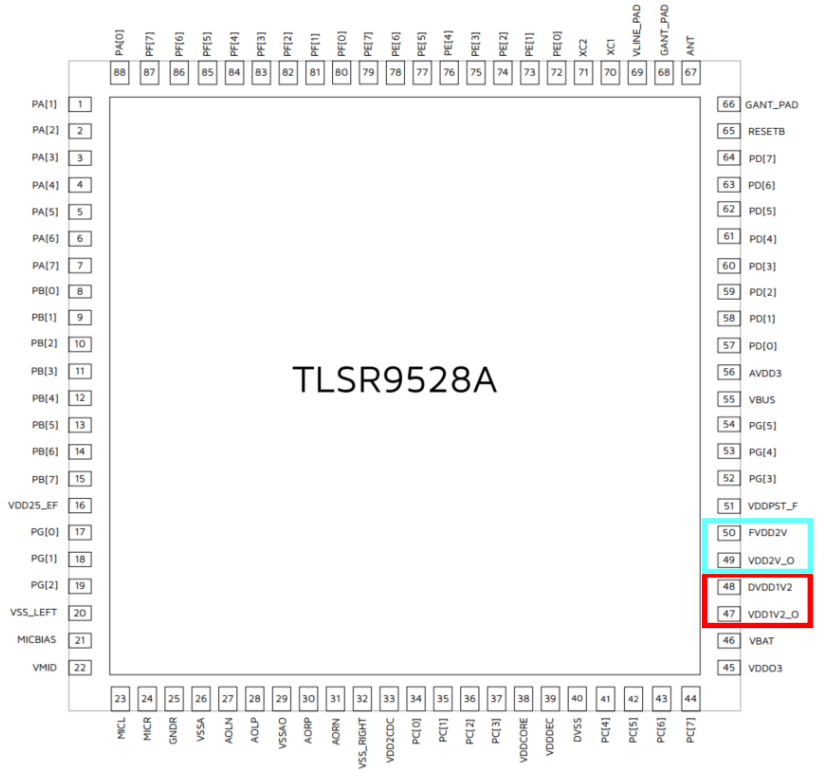
- PIN16(VDD25_EF):
  - Used by E-fuse.
  - A decoupling capacitor, 1uF, is needed.
- PIN22(VMID):
  - Related to embedded codec part in the chip.
  - A decoupling capacitor, 1uF, is needed.
- PIN33(VDD2CDC):
  - Related to embedded codec part in the chip.
  - PIN33(VDD2CDC) is the power supply of embedded codec that a decoupling capacitor, 1uF, is needed. Usually connected to 2V power source.
- PIN38(VDDCORE)/PIN39(VDDDEC):
  - Connected together. And a decoupling capacitor, 1uF, is needed.

Pin layout – Power Supplies : Part B



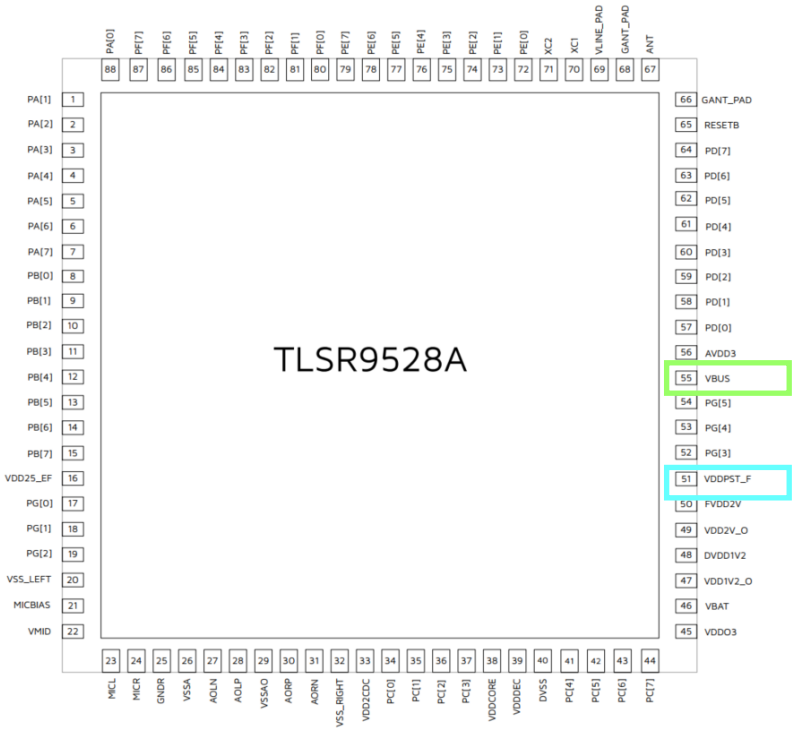
- PIN45(VDDO3)/PIN56(AVDD3):
  - Connected together. And a decoupling capacitor, 1uF, is needed.
  - Power supply for all GPIOs.
  - PIN45 is 3V3 Source, PIN56 is 3V3 Sink.
- PIN46(VBAT):
  - Battery positive terminal. A decoupling capacitor, 1uF, is needed.
  - Lion-battery positive terminal can be directly connected to the pin since voltage range is 1.8V~4.3V.
  - If USB VBUS(5V) is available in application, a external LDO or DCDC is recommended to use for converting USB VBUS(5V) to 1.8V~4.3V for VBAT pin.

Pin layout – Power Supplies : Part B



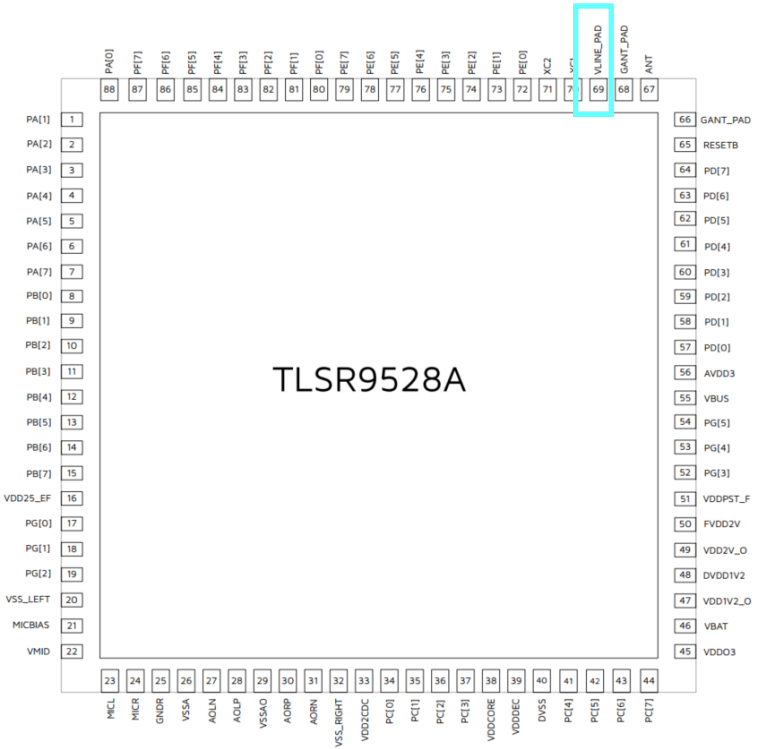
- PIN47(VDD1V2_O)/PIN48(DVDD1V2):
  - PIN47 is 1V2 DCDC Source, PIN48 is 1V2 LDO Source.
  - PIN69 are 1V2 Sink.
  - LDO and DCDC mode are both supported. In real application, DCDC mode is suggested.
  - Some decoupling capacitors are needed.
- PIN49(VDD2V_O)/PIN50(FVDD2V):
  - PIN49 is 2V0 DCDC Source, PIN50 is 2V0 LDO Source.
  - PIN33 are 2V0 Sink.
  - LDO and DCDC mode are both supported. In real application, DCDC mode is suggested.
  - Some decoupling capacitors are needed.

Pin layout – Power Supplies : Part C



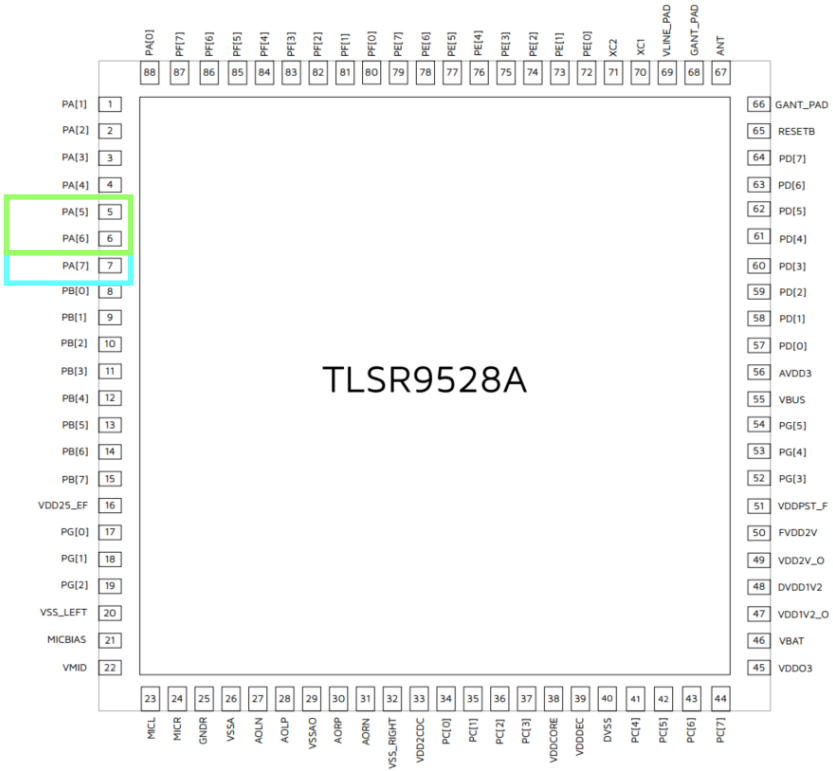
- PIN51(VDDPST_F):
  - PIN51 is internal 1V8 LDO output. And a decoupling capacitor, 1uF, is needed.
  - Power supply for external nor flash.
- PIN55(VBUS)
  - PIN55 is an external power input PIN, the voltage range is 4.5 V ~ 5.5 V. A decoupling capacitor, 1uF, is needed.
  - When use VBUS instead of VBAT supply for TLSR9528A, hardware design should connect VDDO3 with VBAT.
  - When not power from VBUS, don`t connect it to anything.
  - When there is USB plugged in, the VBUS_DET detects that VBUS has power and may generate reset after a few seconds.

Pin layout – Power Supplies : Part D



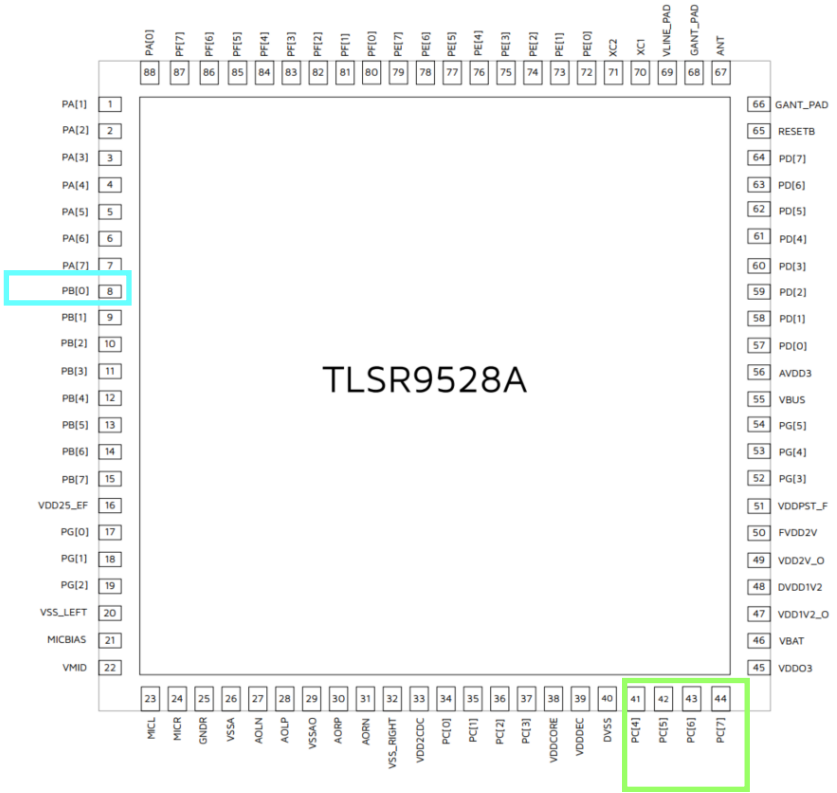
- PIN69(VLINE_PAD):
  - Related to RF part in the chip, power supply for RF part.
  - Decoupling capacitor, 2.2uF&0.1uF, are needed.

Pin layout – Debug Port : Part A



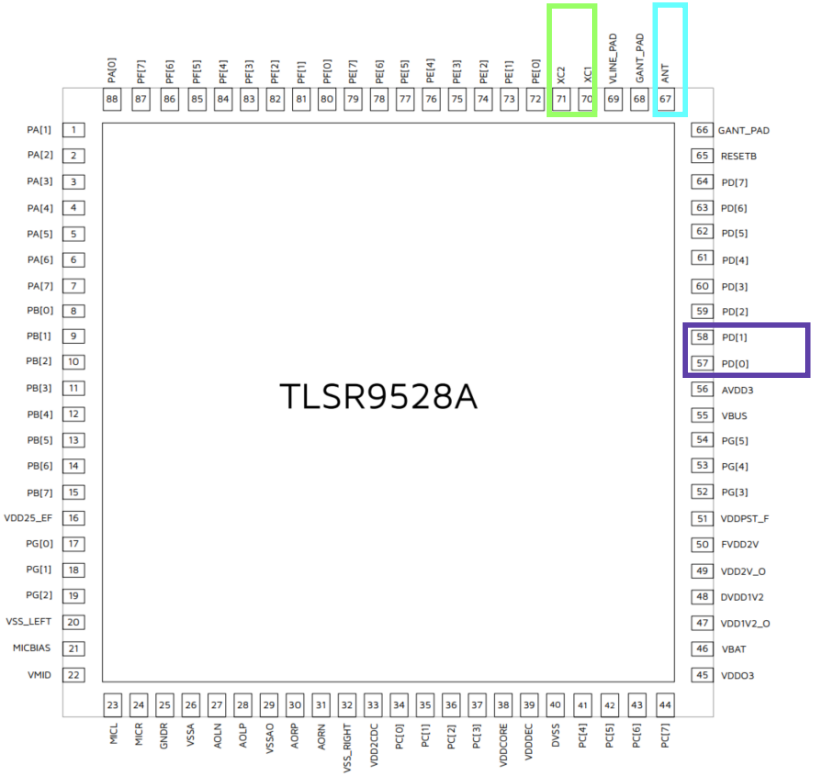
- PIN7(PA7/SWS):
  - Download Pin and must be connected to a test point which is used to download FW.
- PIN5(PA5_DM)/PIN6(PA6_DP):
  - It is USB interface.
  - Recommend to connect to test points for capturing log when FW works.

Pin layout – Debug Port : Part B



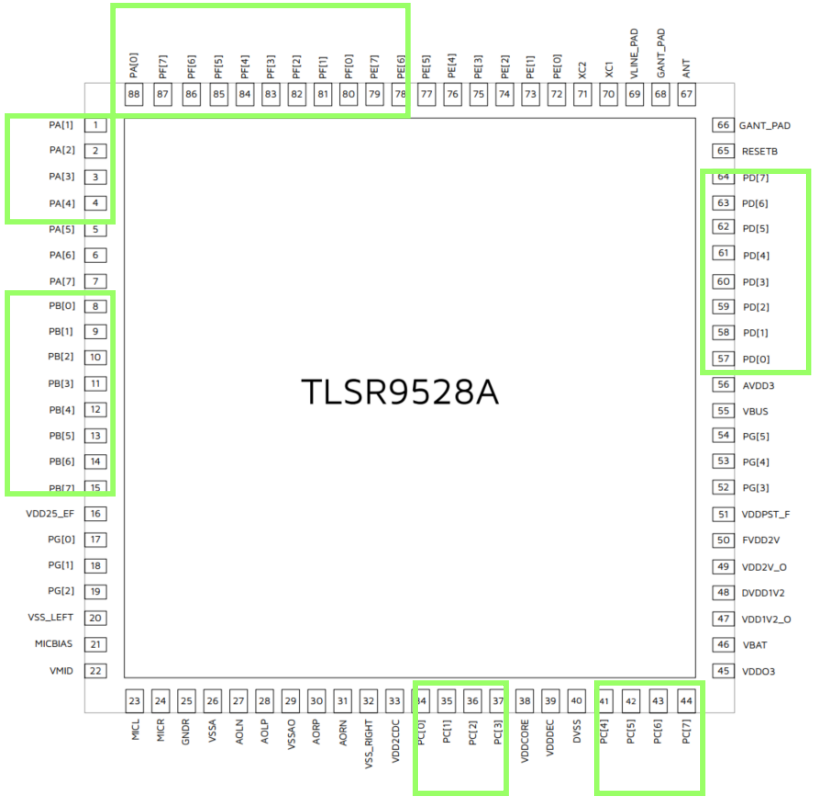
- PIN41/PIN42/PIN43/PIN44:
  - A group of JTAG interface, supports 2-wire(SDP) or 4-wire(JDP) mode.
  - When using SDP, the pins of PC [6] and PC [7] should be used. At this time, PC [4] and PC [5] can be used for other functions.
  - PB[0] is for choosing between SDP & JDP:
    - PB[0] pull-up: SDP
    - PB[0] pull-down: JDP
  - When power on or after coming back from deep sleep mode, SoC will read the PB[0] level, then the debug port is decided. Can not be modified through the init process or register.

Pin layout – RF Part: Part A



- RF Port:
  - PIN67(ANT) is RF port.
  - A 3th-order LC filter is recommend to use for certification. The detail will be introduced in the next page.
- 24Mhz Crystal:
  - PIN70(XC1), PIN71(XC2) connect 24Mhz crystal.
  - Usually recommended specification: 24Mhz – 12pF - +/-20ppm
    - Sometimes try different kind of 24Mhz crystal with different load capacitor, such as 10pf, 15pf because of different PCB layout to get lower frequency offset.
    - For some BLE projects, it is recommended to use the same type of crystal for TX/RX and to verify and calibrate the frequency bias according to different PCBs.
  - The range of internal load capacitor is among 5pF~18pF.
- 32.768K crystal:
  - PD0 and PD1 can be used to connect external 32.768Khz crystal.

Pin layout – RF Part: Part B

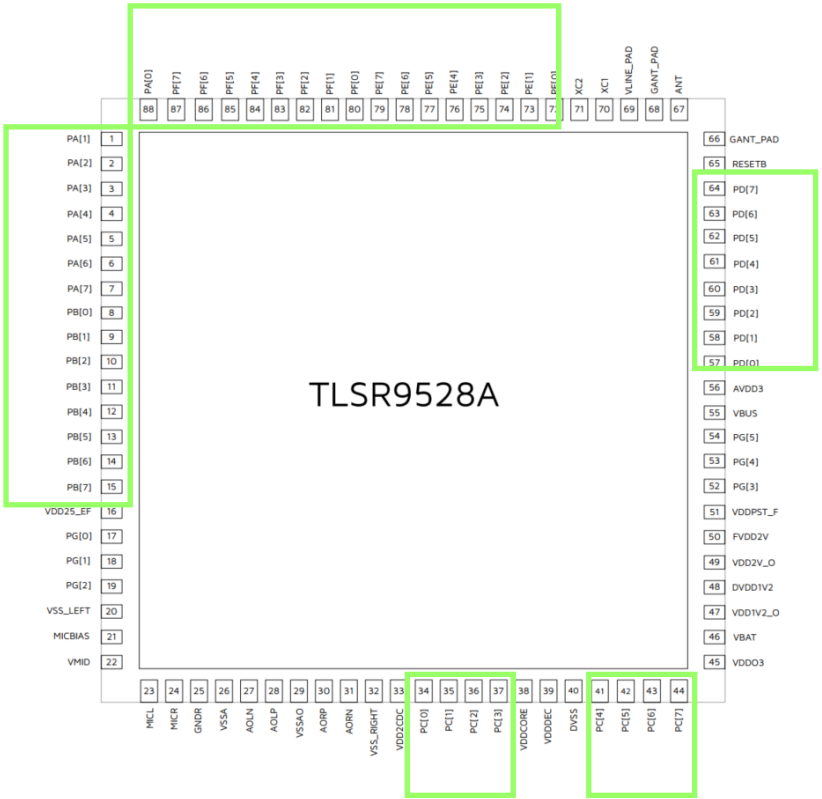


- External FEM Control Port:
  - All GPIOs in the green box can be combined arbitrarily and configured as RX_ CYC2LNA or TX_ CYC2PA
  - TX_ CYC2PA connects TX of external FEM_ EN, RX_ CYC2LNA connects RX of external FEM_ EN

Pin layout – RF Part: Part C

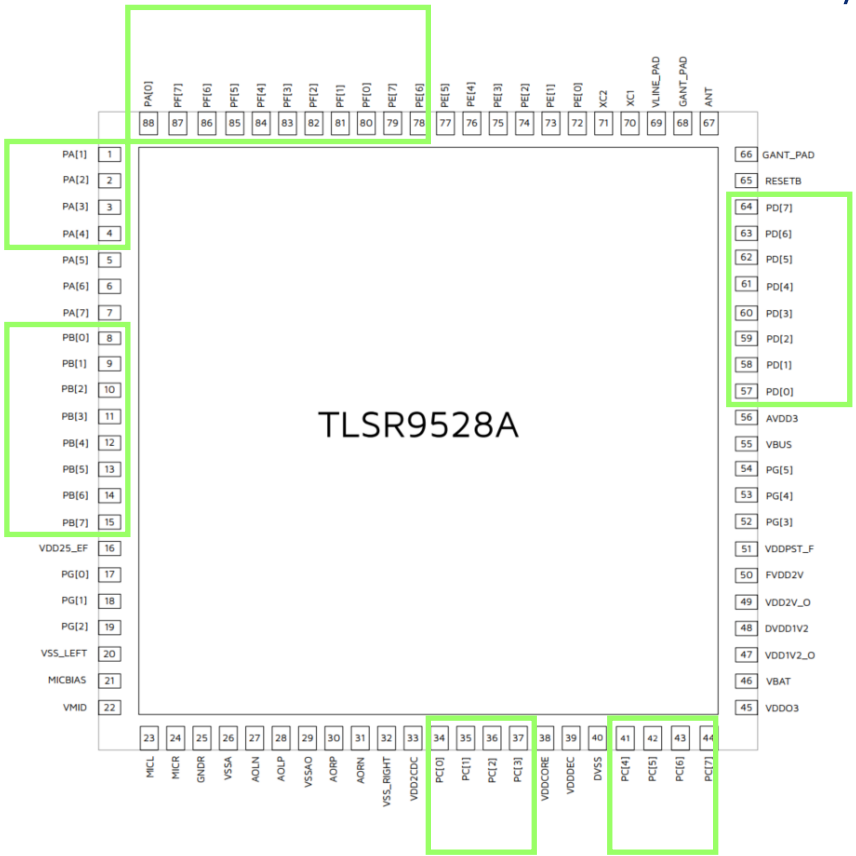
- A 3th-order LC filter is used for matching to pass certification, the values of which are flexibly adjustable corresponding to layout.
- Firstly, use VNA (Vector Network Analyzer) to do RX matching.
  - Customers must power on DUT, and use EMI tool to configure chip into RX mode, then tune RX matching.
- After RX test is finished, SA (Spectrum Analyzer) should be used to check TX harmonic.
  - If harmonics do not meet the requirements, re-do RX matching. Use the VNA to adjust component value to meet the impedance matching requirements, and then check TX harmonic again.
- It is recommend to mount a shielding box on PCBA for certification if customer can afford the cost. It is easy to pass certification and save time.
- TLSR9528A development board has passed FCC certification,
  - FCCID:TBD

Pin layout – GPIO



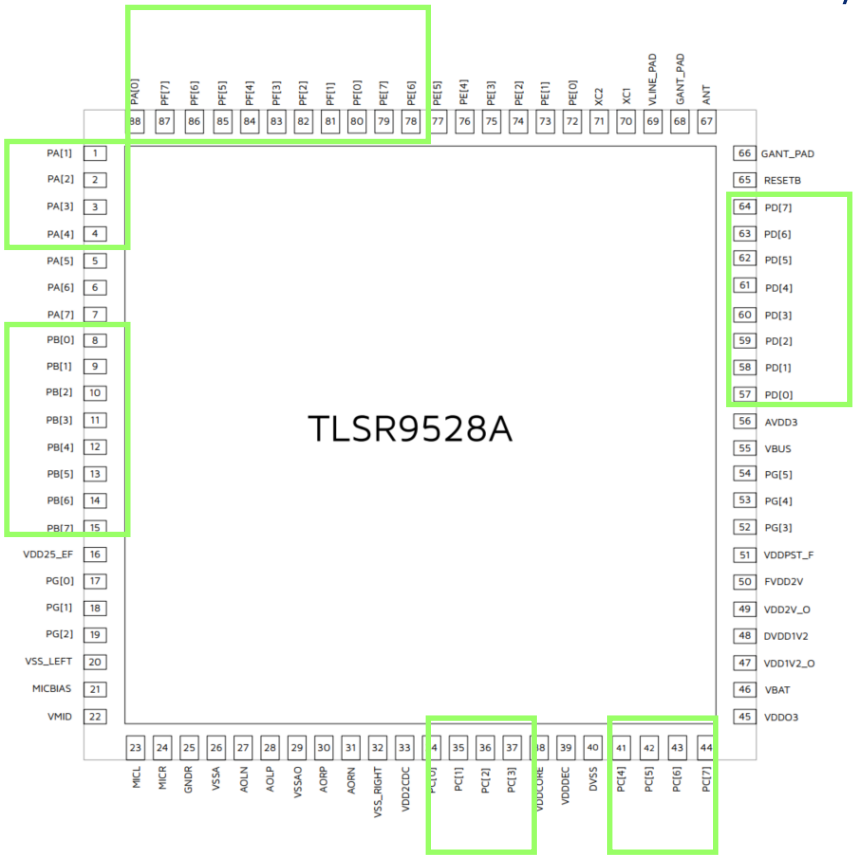
- Refer to chapter 10.1.
- All GPIO pins have configurable pull-up resistor and pull-down resistor.
  - Pull-up resistor: 10K/1M
  - Pull-down resistor: 100K
- All GPIO pins can be independently configured as high-level/low-level wakeup source.
- Two kinds of driving strength:
  - PA[5:7], PE[0:1], PE[4:7], PF[0:7]: maximum=8mA, minimum=4mA
  - Other GPIOs: maximum=4mA, minimum=2mA

Pin layout – PWM



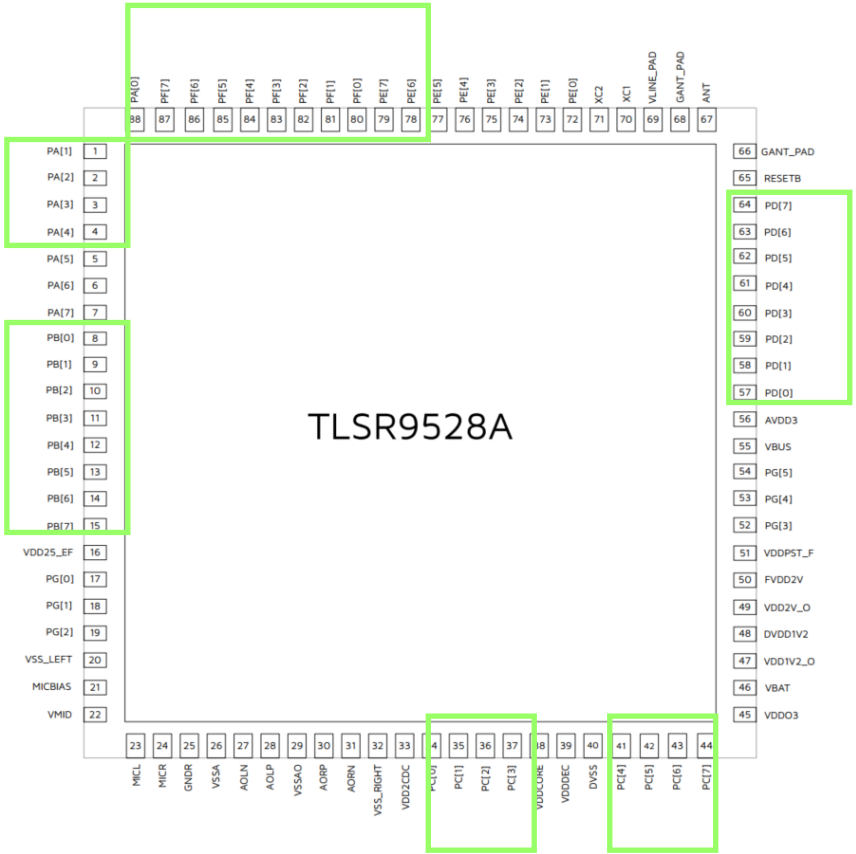
- Supports 6-channel PWM (Pulse-Width-Modulation) output. Each PWM#n (n=0~5) has its corresponding inverted output at PWM#n_N pin
- PWM0 supports five modes, including Continuous mode (normal mode, default), Counting mode, IR mode, IR FIFO mode, IR DMA FIFO mode. PWM1~PWM5 only support Continuous mode.
- Free configuration of any IO as PWM except PA5 to PA7, PE0 to PE5, and PG0 to PG5.

Pin layout – UART



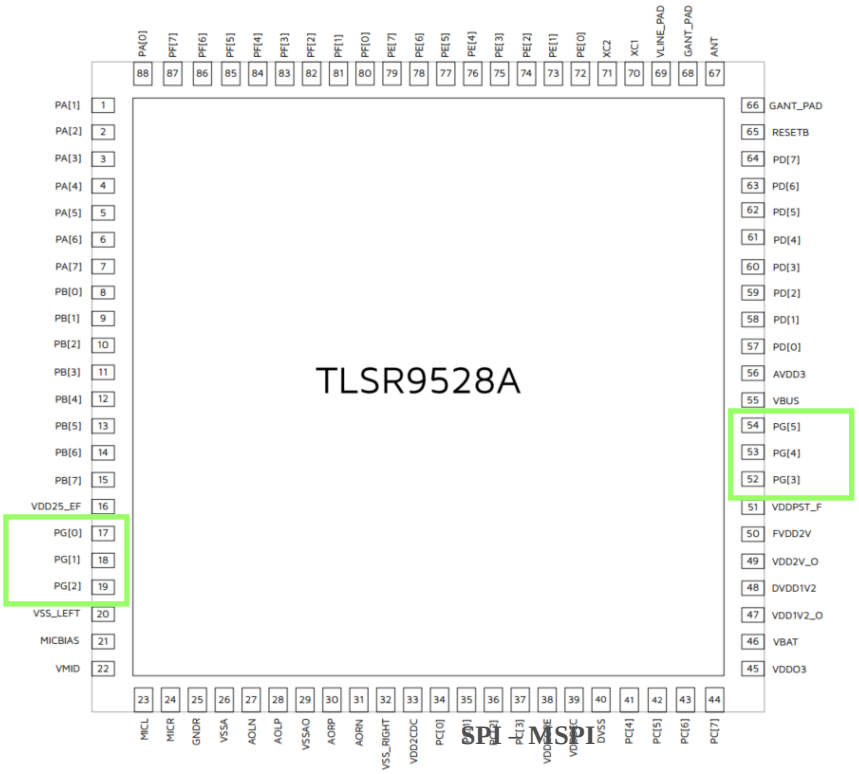
- Supports general UART interface and 7816 UART interface.
- Two groups of UART are supported, UART0 and UART1.
- Free configuration of any IO as UART except PA5 to PA7, PE0 to PE5, and PG0 to PG5

Pin layout – I2C



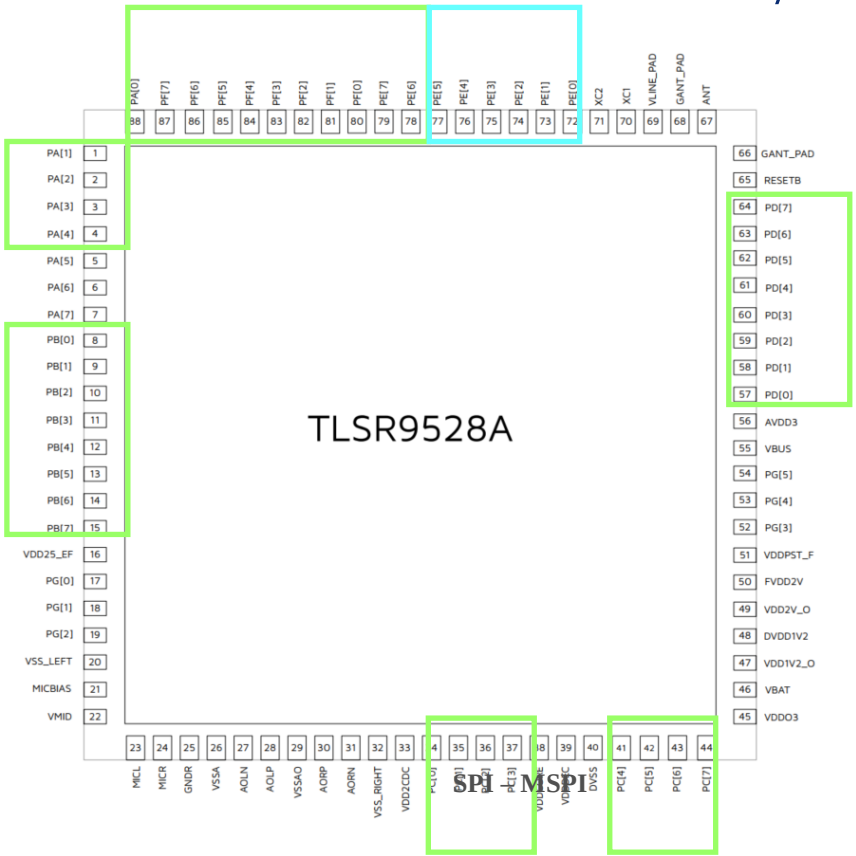
- Support two hardware I2C interfaces, I2C0 and I2C1
- Support I2C Master or Slave mode
- SCK/SDA of I2C0/1: Free configuration of any IO except PA5 to PA7, PE0 to PE5, and PG0 to PG5

Pin layout – SPI : Part A



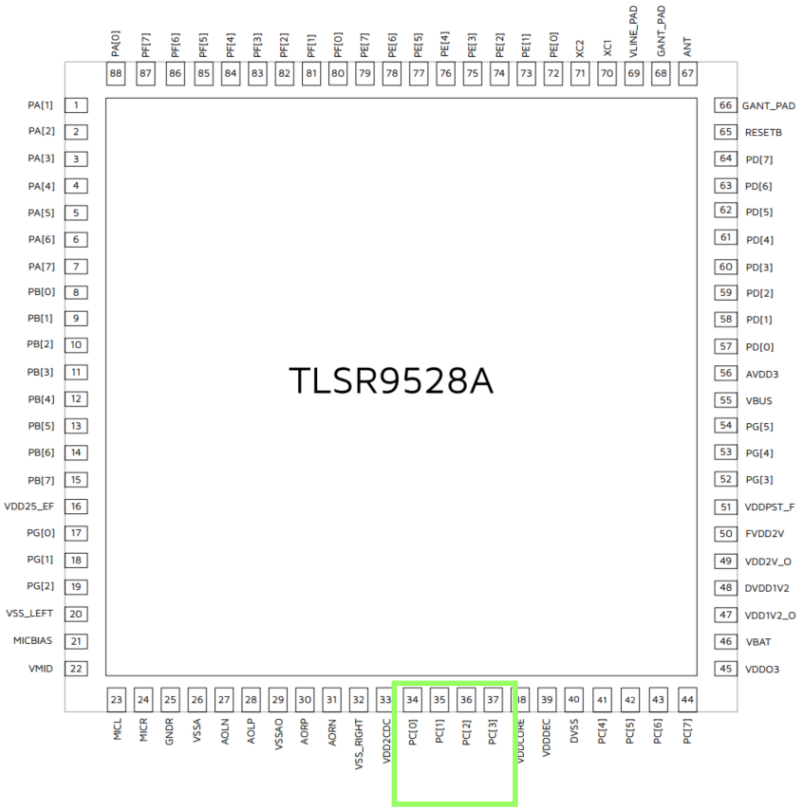
- Support MSPI/GSPI/LSPI/SSPI four SPI interfaces
- Rate support
  - MSPI: Single -line fastest rate to 64Mbps
  - GSPI: Single -line fastest rate to 48Mbps
  - LSPI: Single -line fastest rate to 48Mbps
  - SSPI: Single -line fastest rate to 24Mbps
- SPI – MSPI
  - MSPI connected to nor Flash
    - MOSI:PG0
    - CK:PG1
    - IO3:PG2
    - CN:PG3
    - MISO:PG4
    - IO2:PG5

Pin layout – SPI : Part B



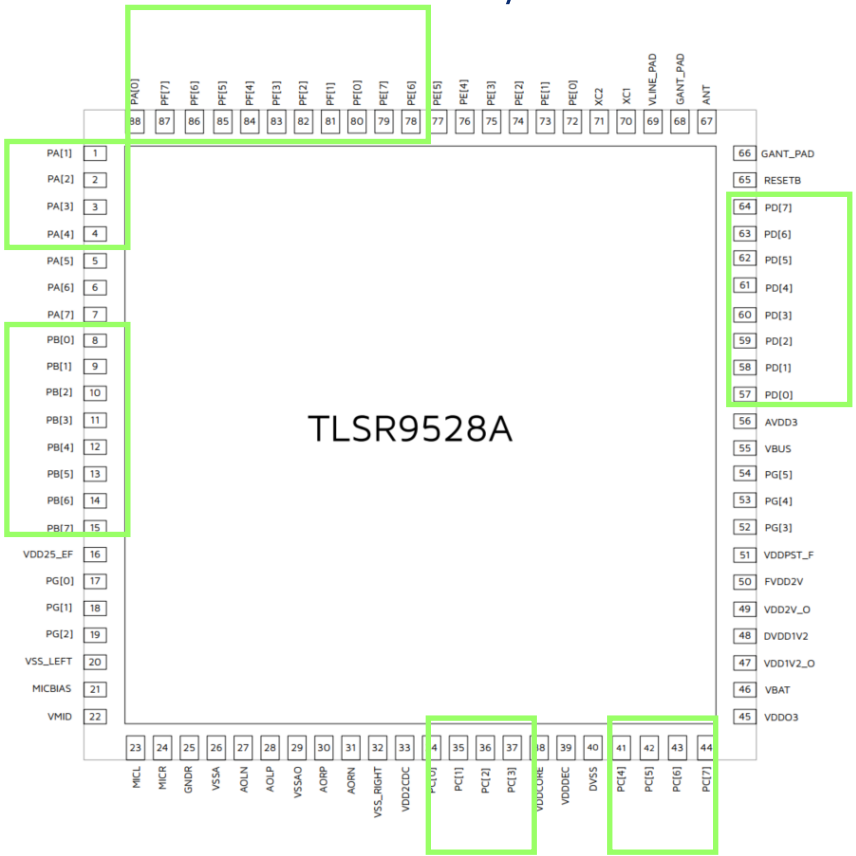
- SPI – GSPI
  - GSPI is a high -speed application, which can connect PSRAM or NAND, support master or slave mode
    - Free configuration of any IO as GSPI except PA5 to PA7, PE0 to PE5, and PG0 to PG5
- SPI – LSPI
  - LSPI can be connected to LCD and supports master or slave mode
    - CN:PE0
    - CK:PE1
    - MOSI:PE2
    - MISO:PE3
    - IO2:PE4
    - IO3:PE5

Pin layout – SPI : Part C



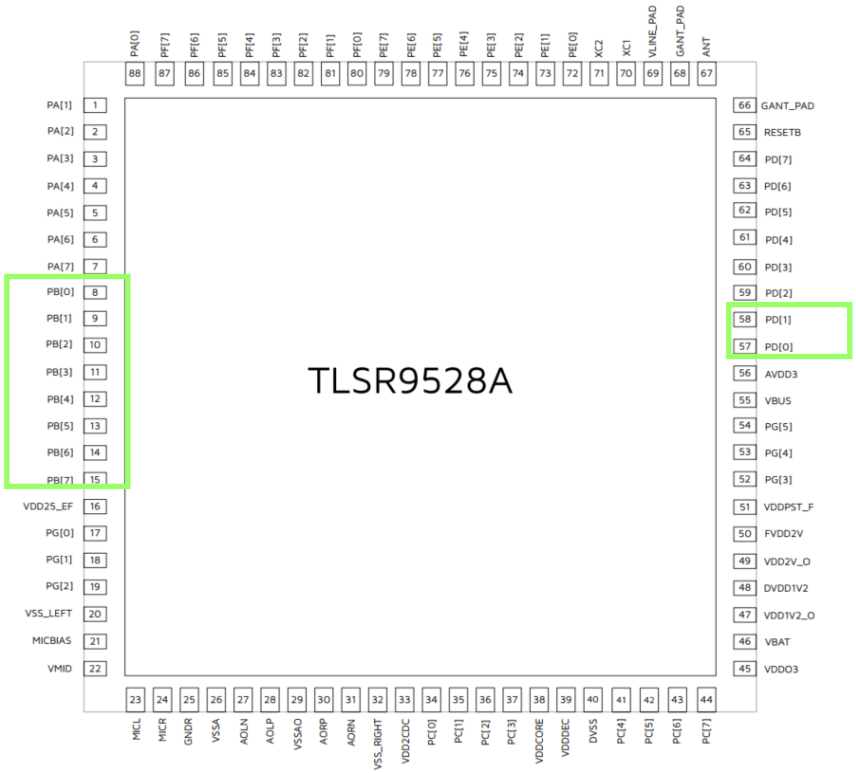
- SPI – SSPI
  - SSPI only support slave mode
    - CN:PC0
    - CK:PC1
    - SI:PC2
    - SO:PC3

Pin layout – RF front-end & Antenna Select Pins



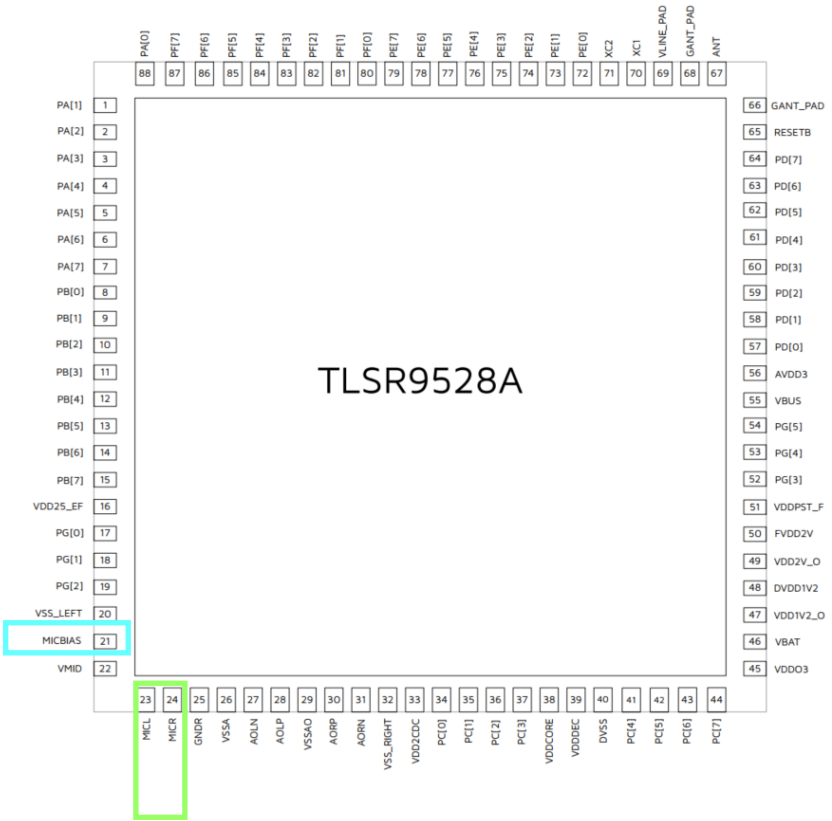
- External RF front-end Pins:
  - TXCYC is used to control the PA (Power Amplifier) of external RF Front-end.
  - RXCYC is used to control the LNA of external RF Front-end.
  - Free configuration of any IO as TXCYC/RXCYC except PA5 to PA7, PE0 to PE5, and PG0 to PG5
- Antenna Select Pins:
  - One groups of SEL<0:3> are used to select one of up to sixteen external antennas. The selected antenna channel is connected to the RF_IO pin.
  - Free configuration of any IO as ATSELx except PA5 to PA7, PE0 to PE5, and PG0 to PG5

Pin layout – ADC Pins



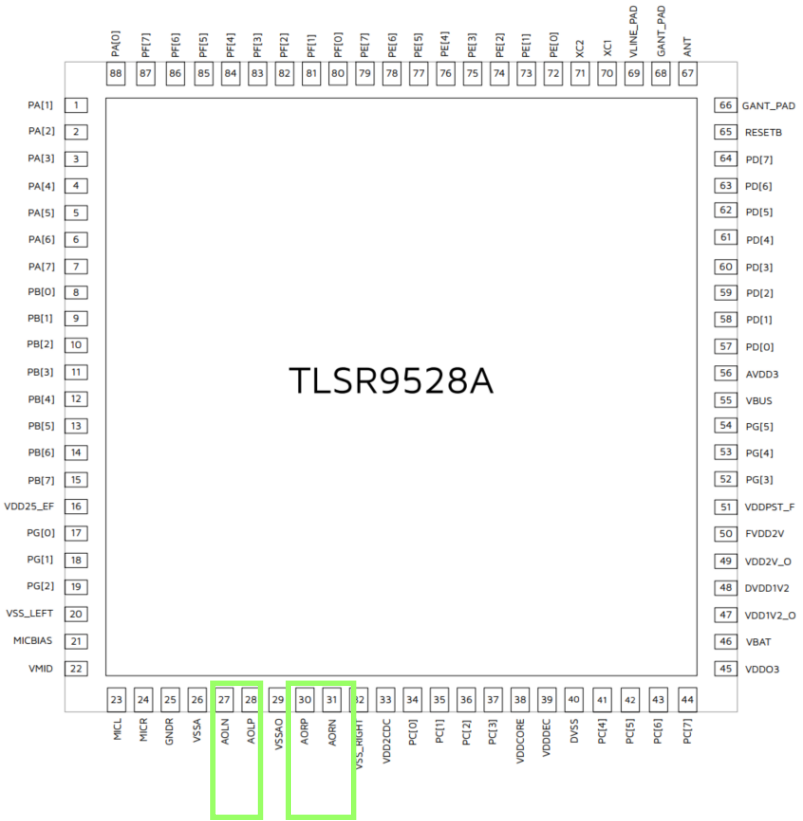
- ADC:
  - Supports up to 10 detect pins, including PB0~PB7, PD0~PD1.
- Battery voltage detection:
  - For applications where the power supply is below 3.6V, the battery can be connected directly to the VBAT pin, but this method has a lower detection accuracy. Recommended ADC for battery voltage detection
  - For applications where the power supply is above 3.6V, the battery can only be connected to an ADC detection pin for voltage detection through a voltage divider resistor.
  - If the system is powered by only one AAA batteries, it needs to be connected to a boosted DCDC. Then use Vbat direct detection or ADC detection for voltage detection

Pin layout – Audio Part: Part A



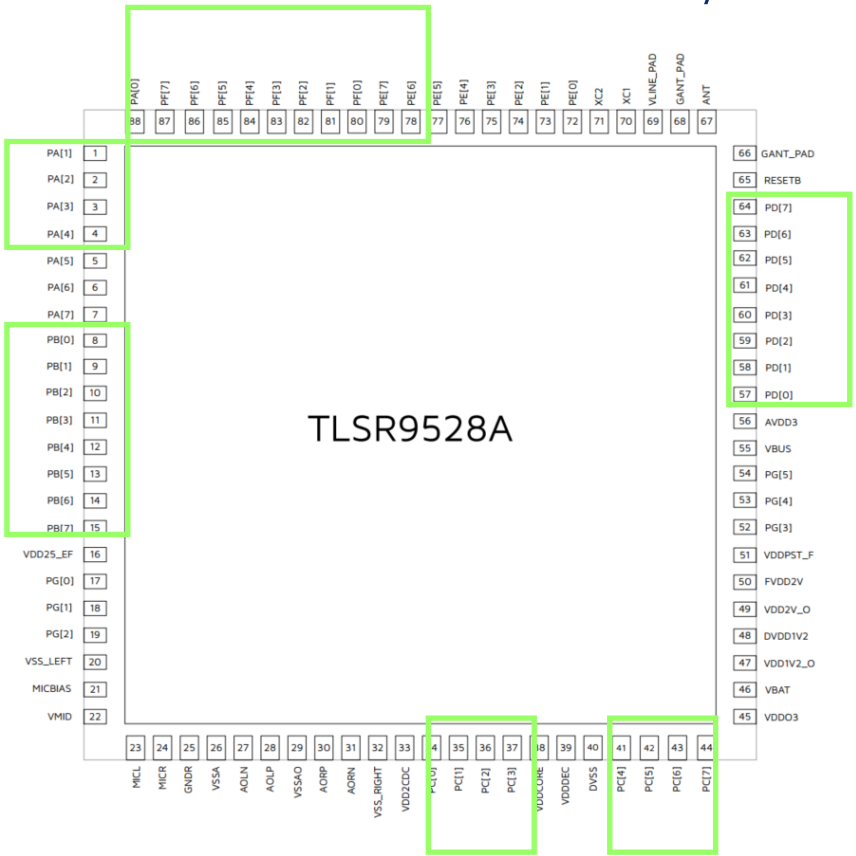
- Internal Audio Codec:
  - Audio input path - AMIC:
    - Supports 2 channels, only single mode.
      - PIN23(MICL) are channel 1, higher priority.
      - PIN24(MICR) are channel 2.
    - PIN21 (MICBIAS) is the microphone power supply pin.

Pin layout – Audio Part: Part B



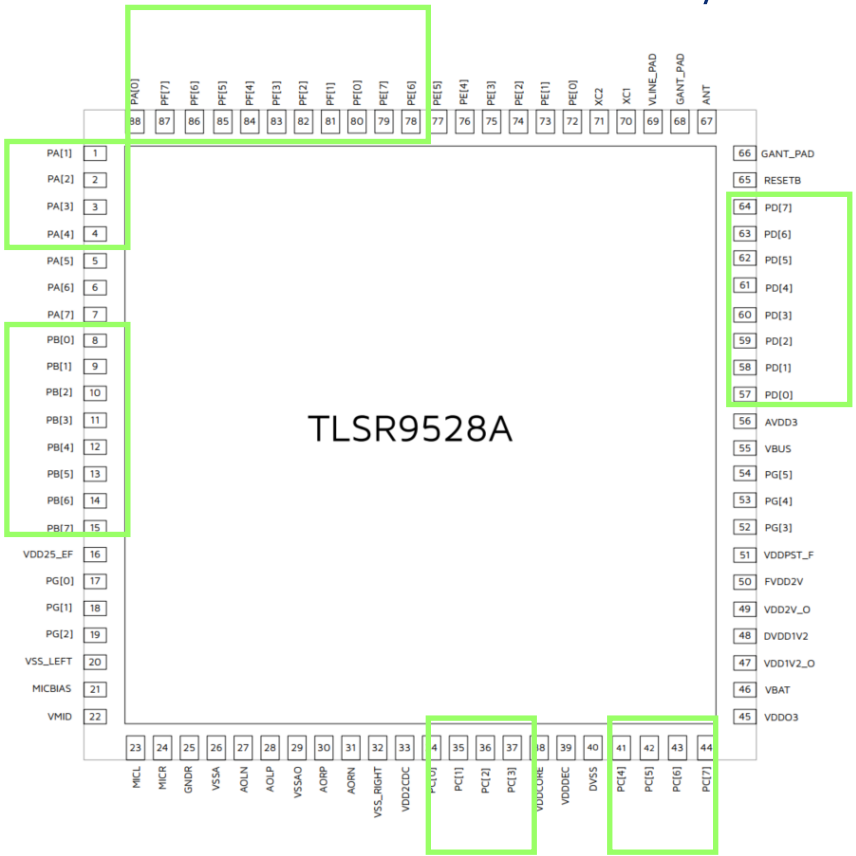
- Internal Audio Codec:
  - Audio output path:
    - Supports 2 channels, differential mode.
      - PIN27(AOLN)/PIN28(AOLP) are L channel.
      - PIN30(AORP)/PIN31(AORN) are R channel.
    - For headset applications support 16ohm and 32ohm speakers. For watch application needs to add audio PA.
    - Single ended output is not recommended
      - There is a DC bias on the single ended signal line, and a DC isolation capacitor needs to be added to connect to the speaker.
      - The voltage amplitude of the single ended output signal is low, which is half of differential output.

Pin layout – Audio Part: Part C



- DMIC:
  - Supports two digital microphones (DMIC0 and DMIC1)
    - DMIC0 – Data/Clk0:
      - Free configuration of any IO as Data/Clk0 except PA5 to PA7, PE0 to PE5, and PG0 to PG5
    - DMIC1 – Data/Clk1:
      - Free configuration of any IO as Data/Clk1 except PA5 to PA7, PE0 to PE5, and PG0 to PG5

Pin layout – Audio Part: Part D

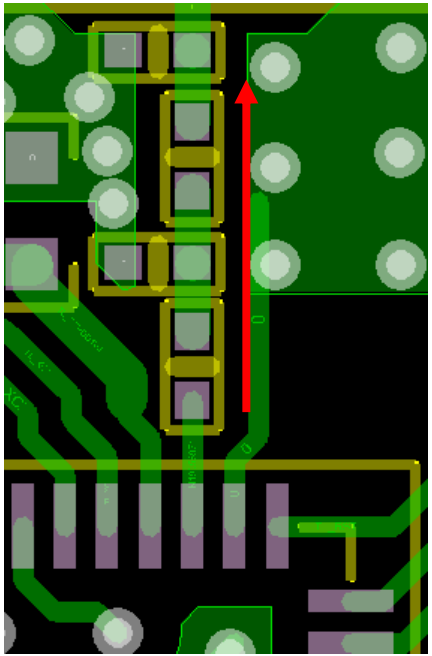


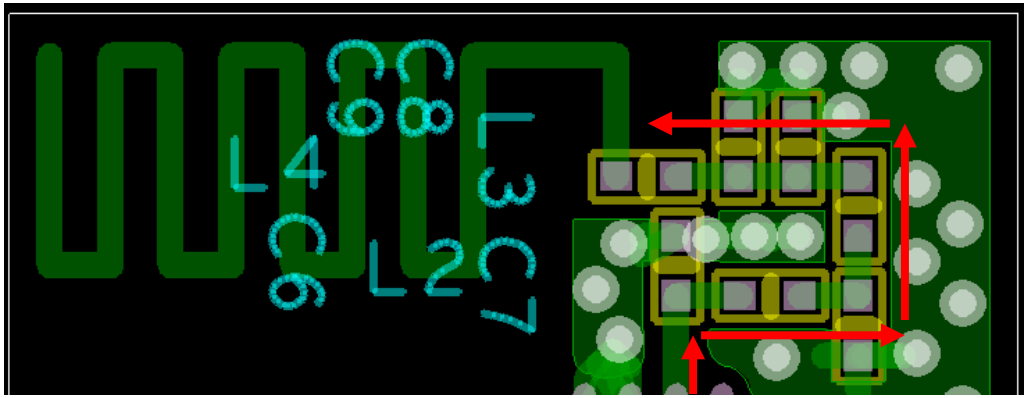
- I2S interface:
  - Supports two I2S interfaces (I2S0 and I2S1)
  - I2S PINs
    - When working in 5-wires mode,
      - bit clk
      - output frame clk
      - output data
      - input frame clk
      - input data
    - When working in 4-wires mode,
      - bit clk
      - output frame clk
      - output data
      - input data
  - I2S pins can be configured in any combination except for PA5 to PA7, PE0 to PE5, and PG0 to PG5

PCB Design Guideline

RF layout

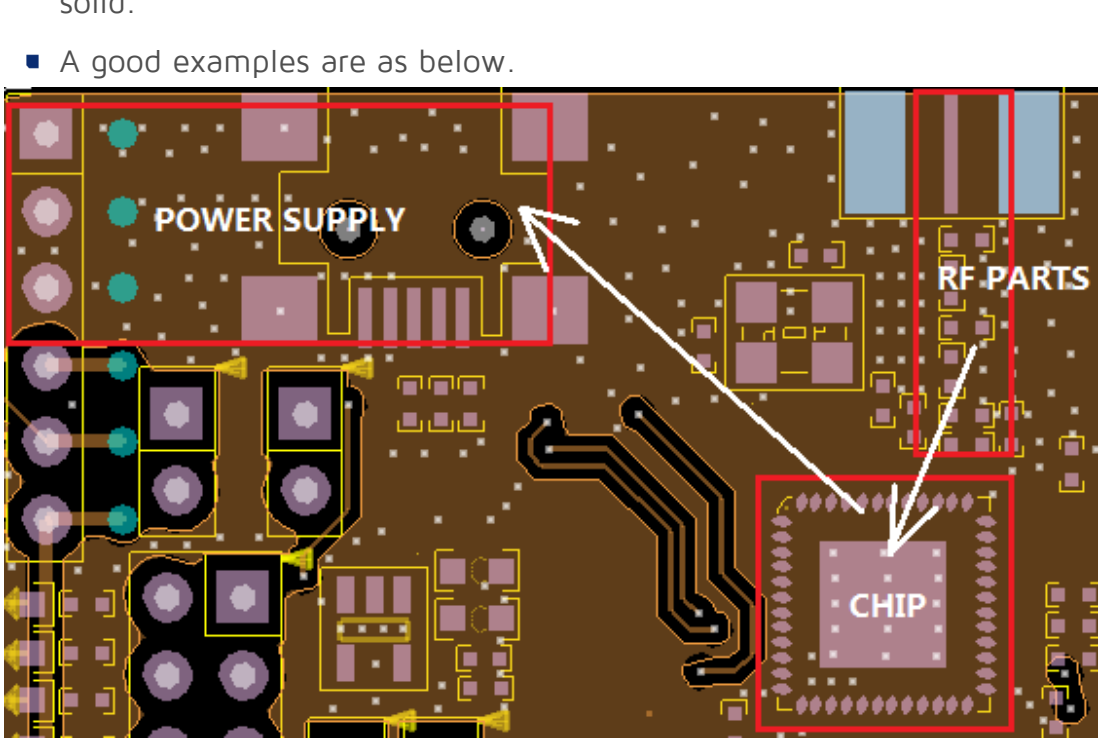
- The components on the RF path MUST be placed one by one. and they MUST be placed close to each other, no stub.
- It the area is not enough, can fold it, but MUST use ground and via to shield RF trace.

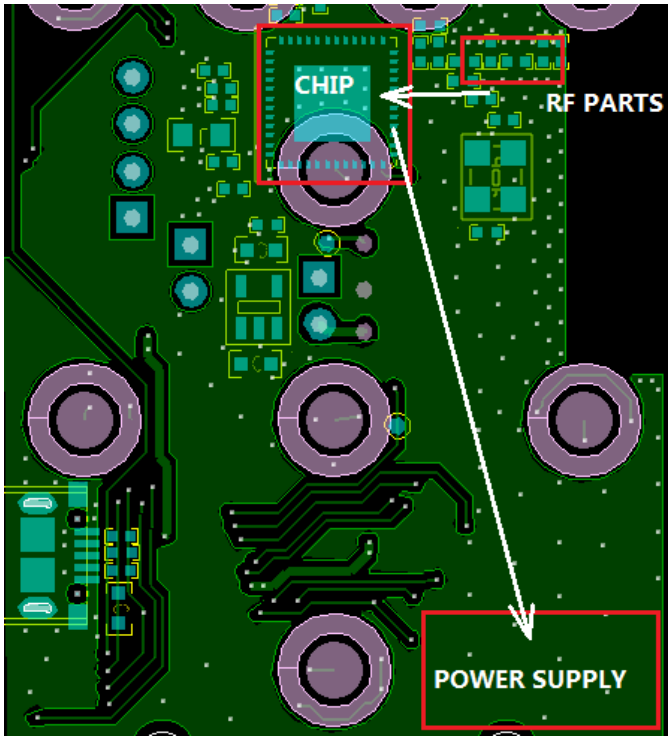




Solid Ground Plane

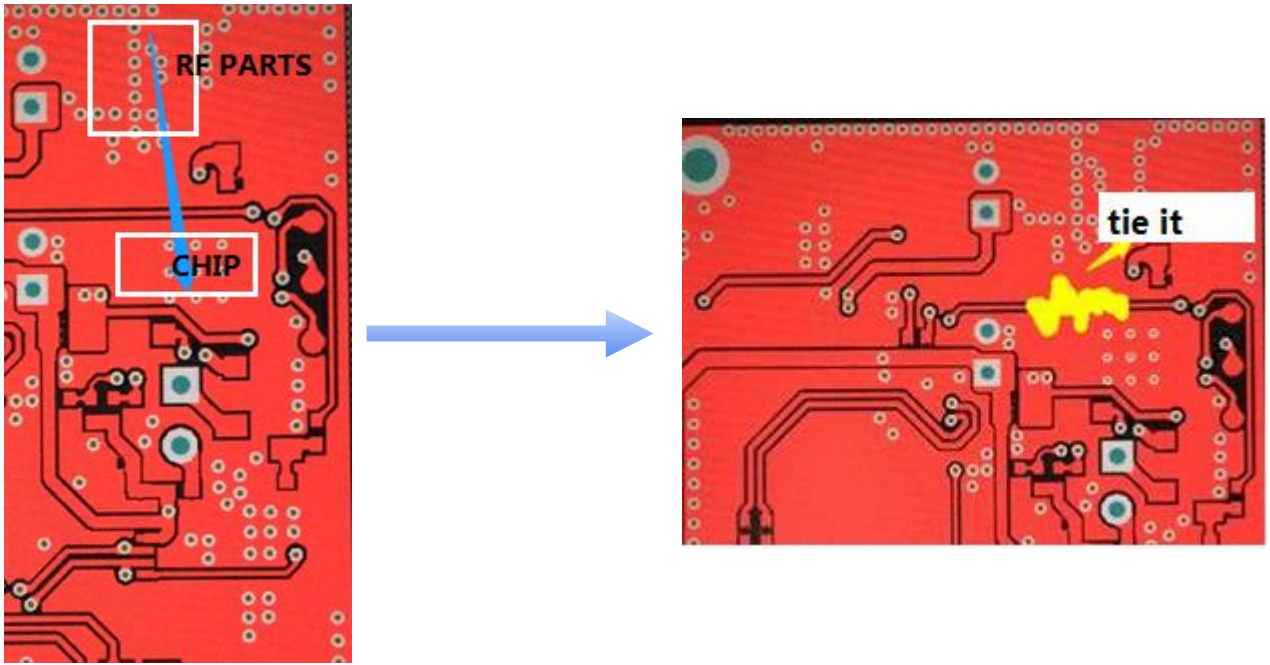
- The ground plane MUST be wide, solid. The ground plane from power supply to chip, then at last to RF parts MUST be solid.
- A good examples are as below.





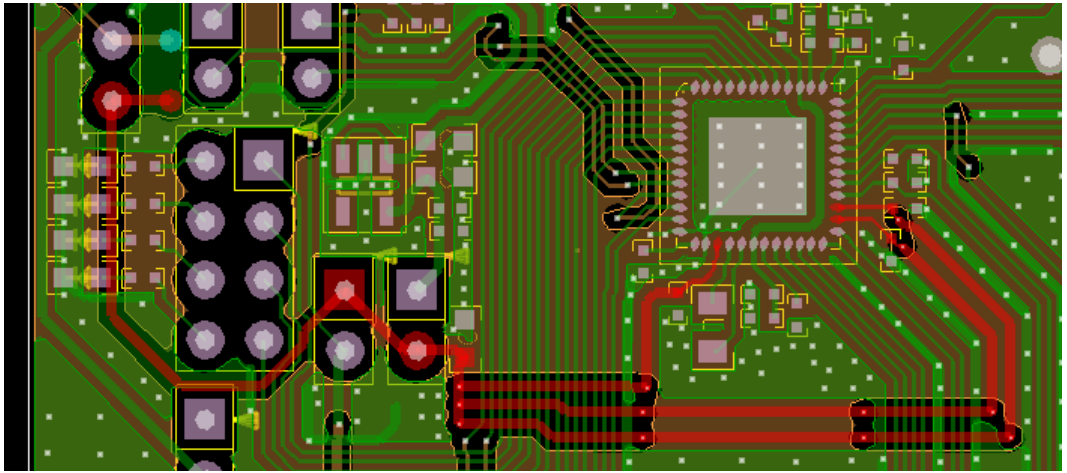
Solid Ground Plane(Cont)

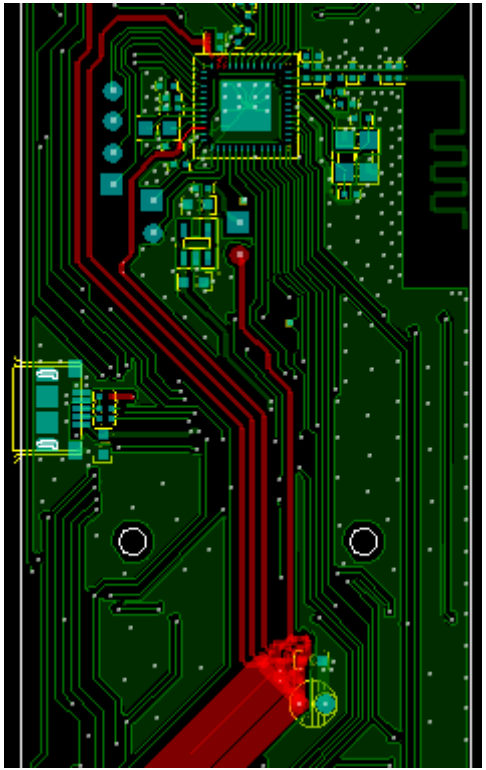
- A bad example is as below.
  - Ground plane between RF parts and chip is cut off, the rx performance is greatly affected.
  - Tie them together, the RX performance matches the data on the datasheet.



Star connection

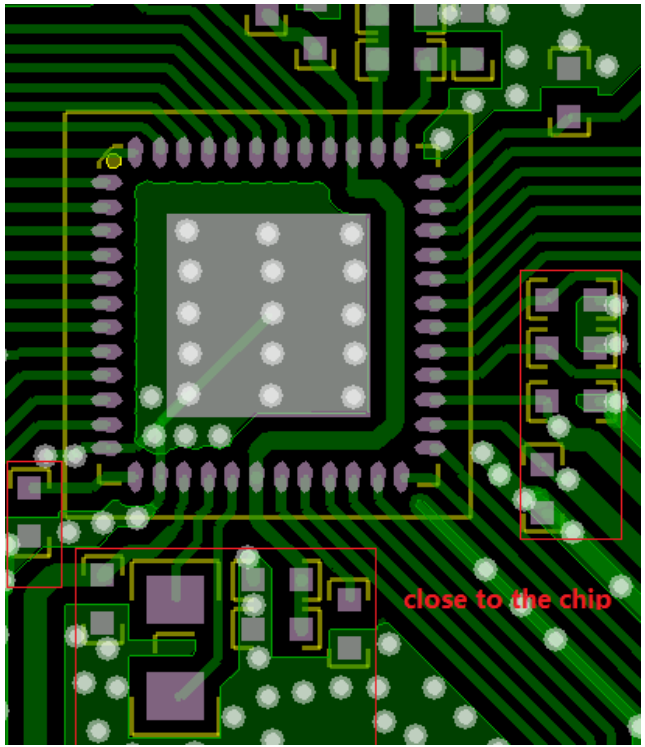
- Power supply should be connected in star-type connection.
  - If there is no audio function, can connect them together.

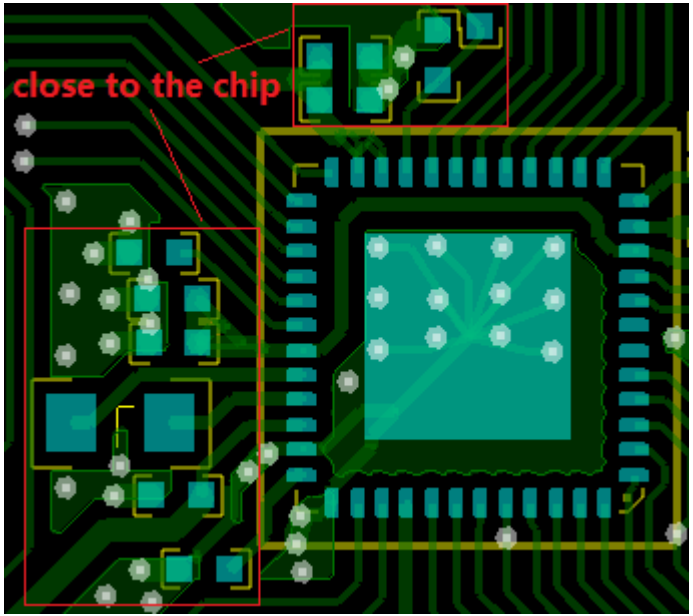




Decoupling capacitor

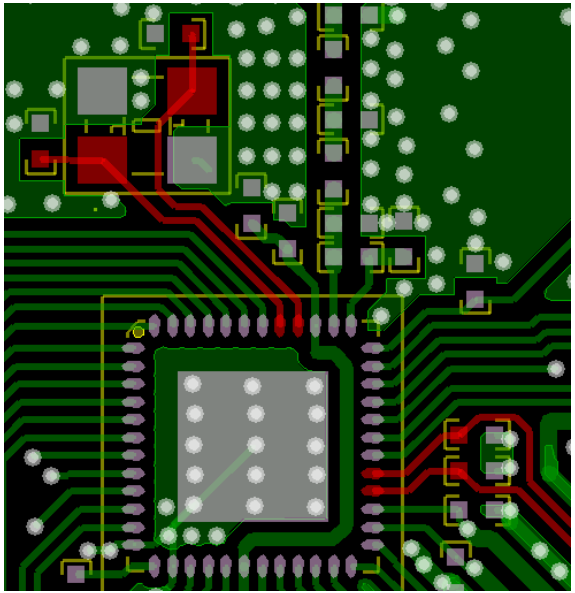
- Decoupling capacitors MUST be placed close to power pins.

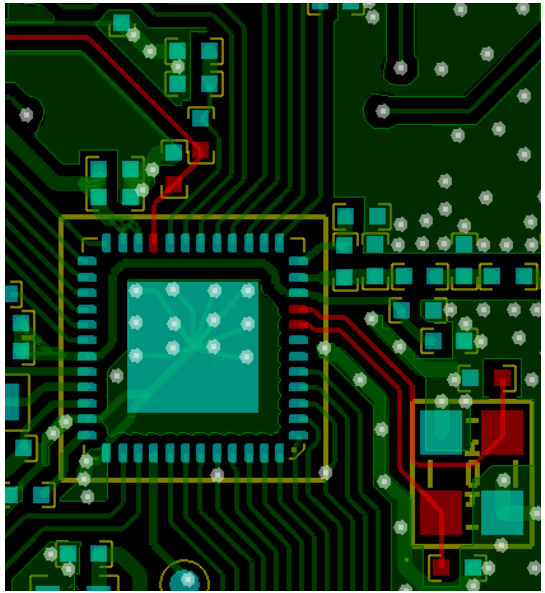


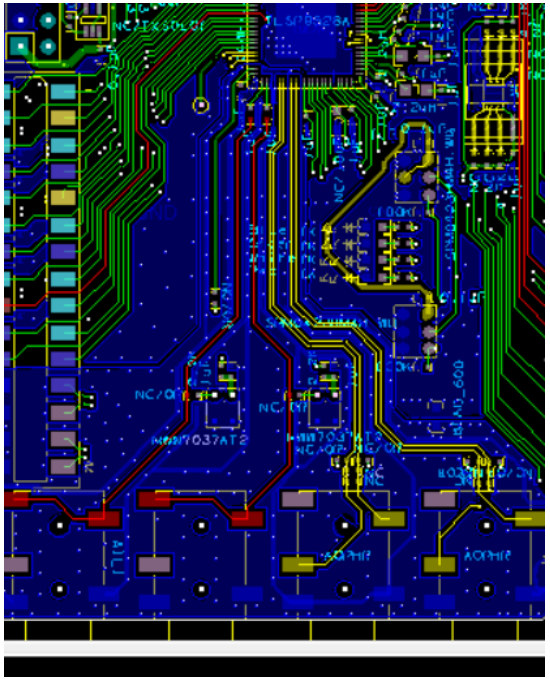


Key traces

- To avoid EMI issue, some important parts such as crystal, audio trace, mic trace and usb trace MUST be shielded by GND and via.

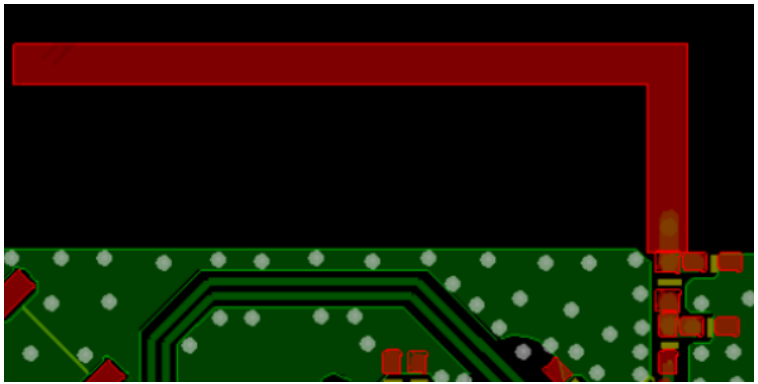






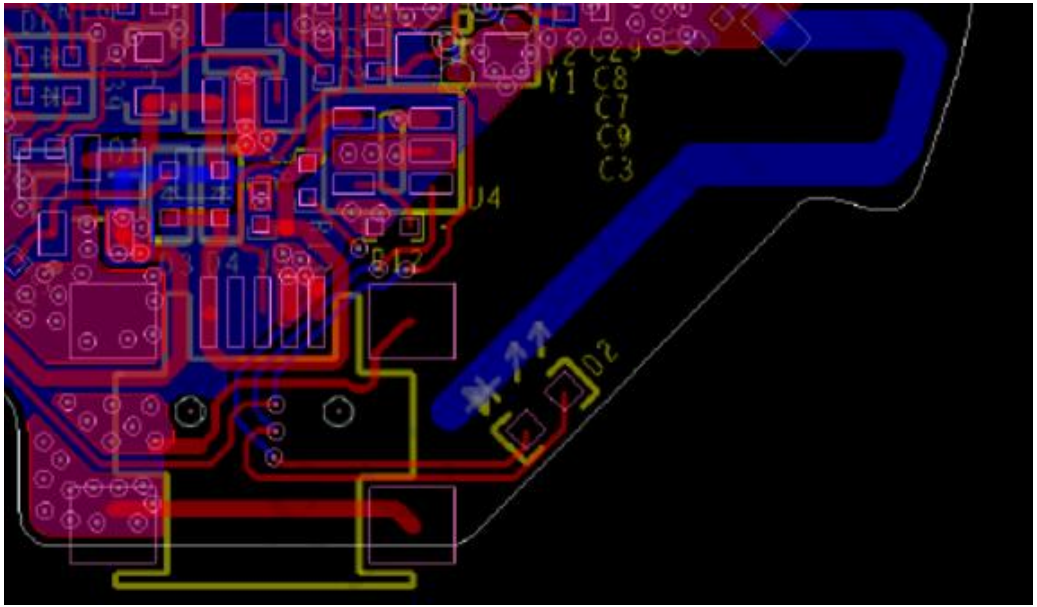
Antenna – common requirement

- Antenna trace width shouldn`t be too narrow in order to decrease loss.
- Line width should be 0.5mm or above, generally it`s recommended to be 0.5mm or 1mm.
- Top and bottom of antenna location should not be covered by GND.
- The distance between antenna and GND should be 3mm or above.
- Generally antenna length is 20mm~30mm. The smaller the GND is, the longer the antenna should be.



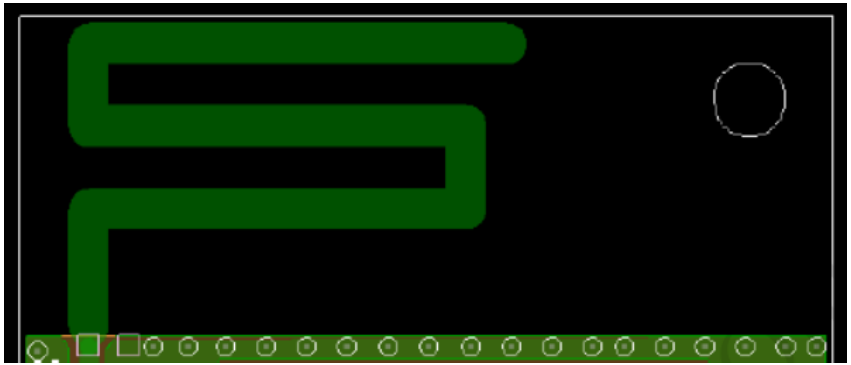
Antenna – keep away others

- Keep PCB antenna far away from metal, battery, or other components, such as 3mm or 5mm.
- A bad example is showed as below. The antenna is too close to USB connector.



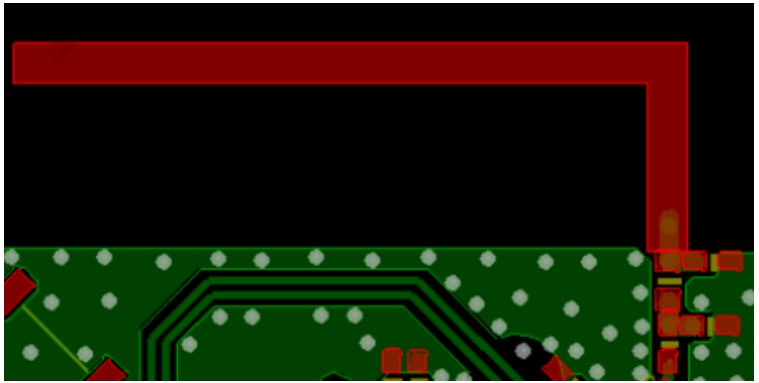
Antenna – don`t exposed to others

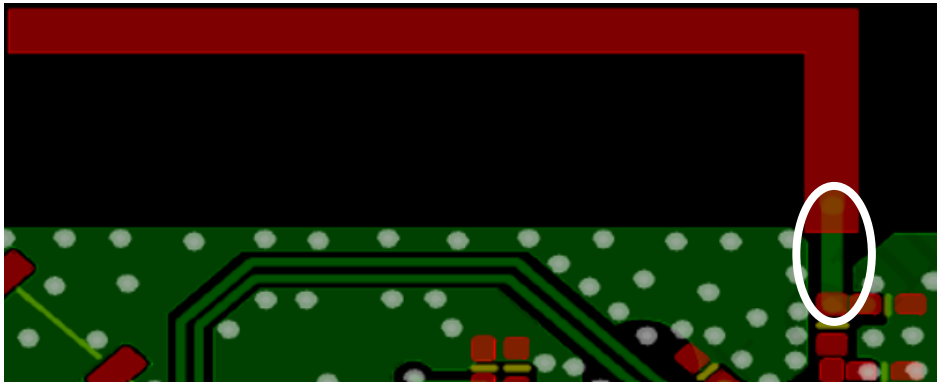
- There MUST be a row of via holes along the antenna on the side parallel to GND. Do not directly expose trace or pad to the antenna.
- The left is a good example. The right is a bad example.



Antenna – matching components

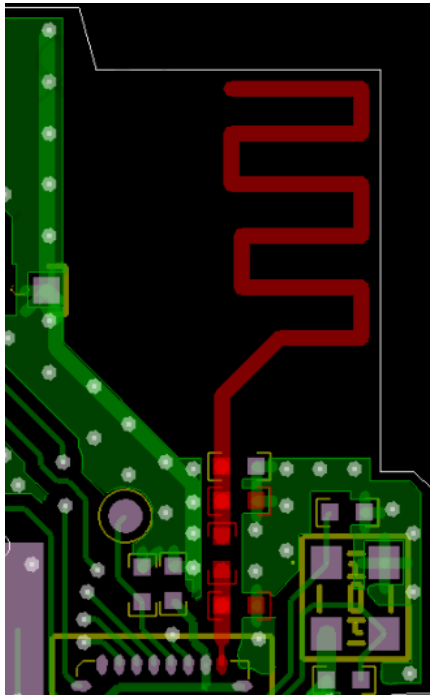
- Antenna matching components should be placed at the boundary of antenna and GND without shrink inward or expand outward.
- The left is a good example. The right is a bad example.

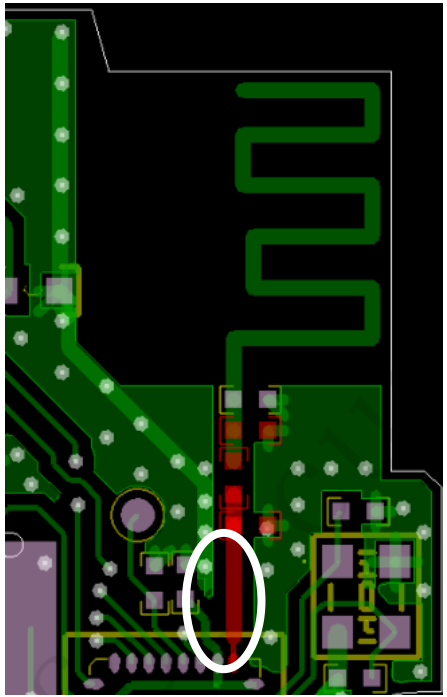




Antenna – impedance design

- The RF line to the antenna port should be short. If RF trace can`t be designed shortly, it must be designed as 50ohm micro-strip line.
- The left is a good example. The right is a bad example.

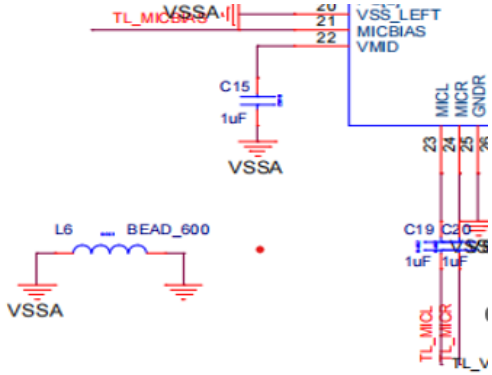




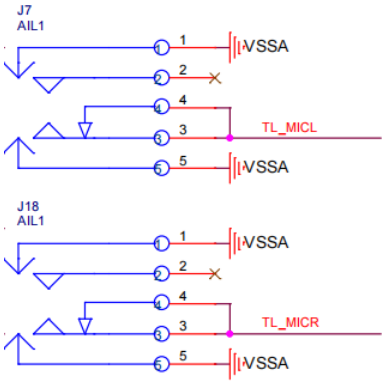
Audio Design Guideline

Audio Input – Codec

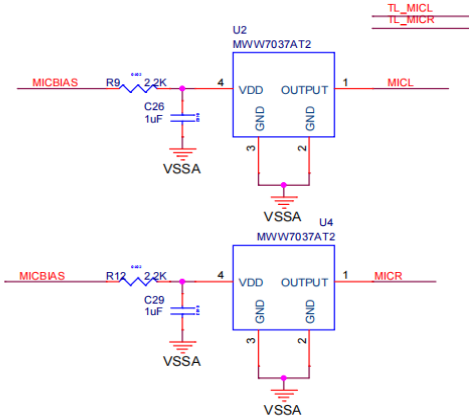
- Support two audio input channels, MIC_L has a higher priority.
- Only support single-ended inputs
  - Chip site: MICL or MICR series connected 1uF capacitor.
  - LINE_IN: This method can be connected to a single input 3.5 mm audio jack.
  - MEMS MIC: MICBIAS needs attention to add filtering.



Chip Site



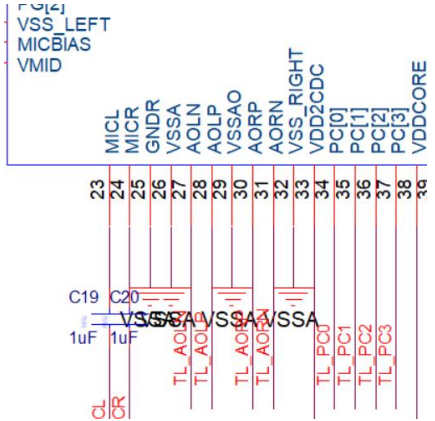
LINE_IN Connection

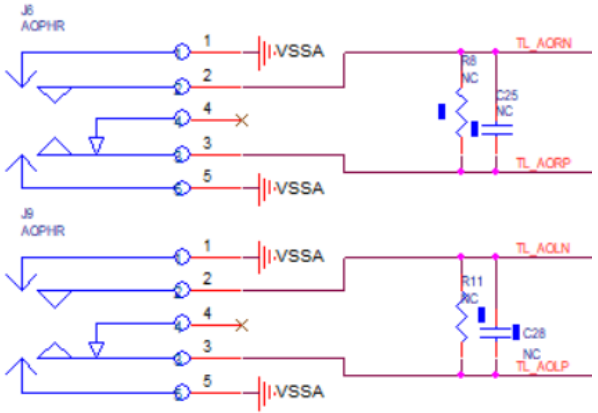


MEMS MIC connection

Audio Output – Codec

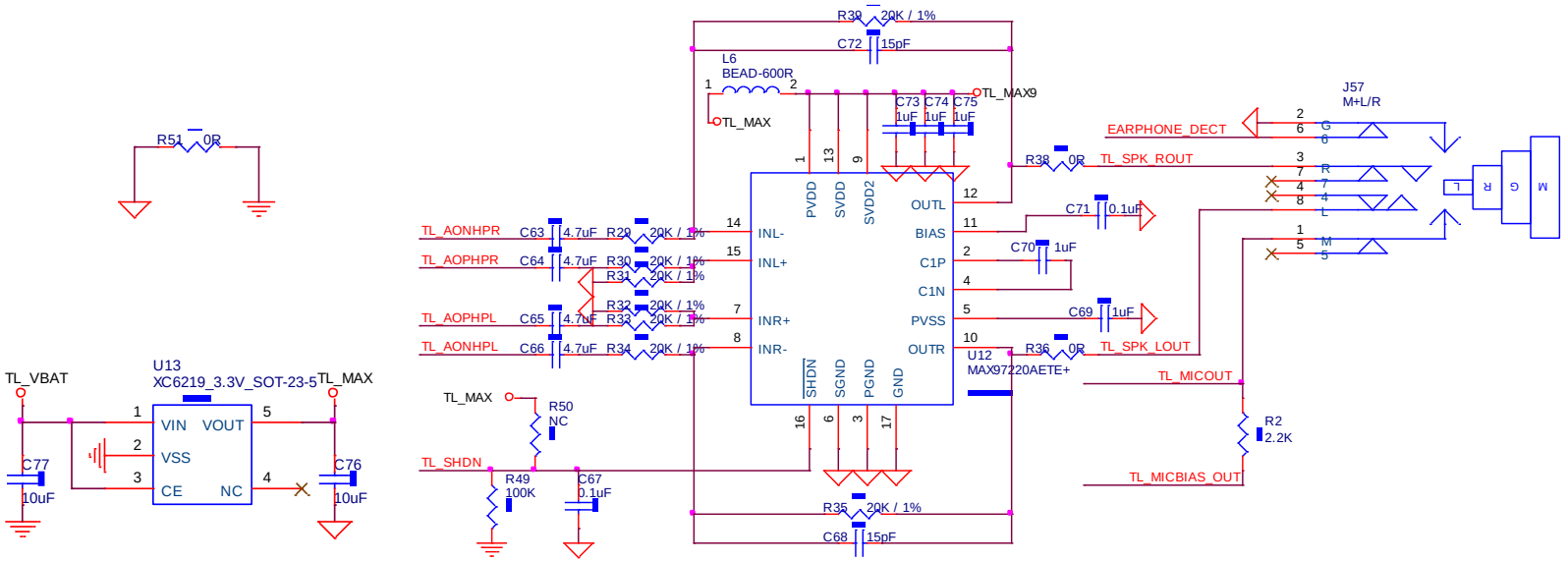
- Audio support stereo channel output, only support differential connection
  - AOLP and AOLN are the positive and negative poles of the audio left channel output.
  - AORP and AORN are the positive and negative poles of the audio right channel output.
  - The left and right channels are connected to the speakers, supporting 16ohm and 32ohm load.





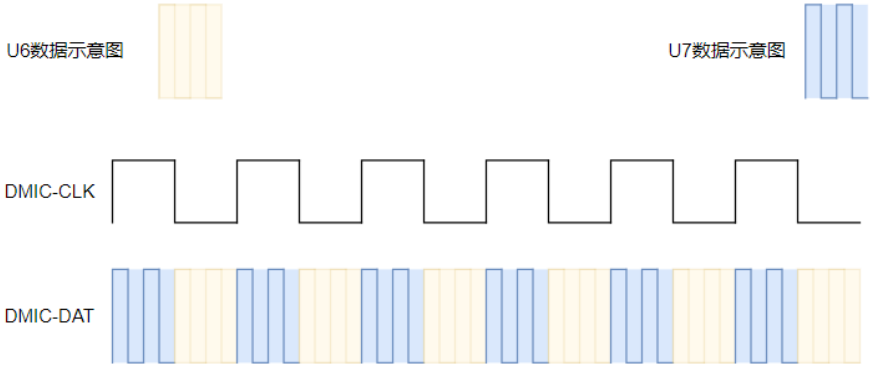
Audio Output – Codec

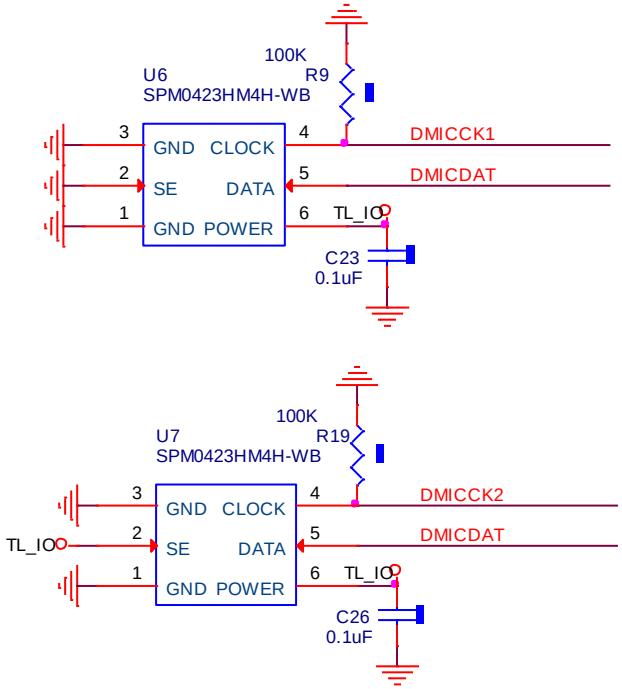
- Single-ended audio output, requires additional differential to single-ended chip
- Differential to single-ended part of the analog ground and chip ground with 0R resistor for isolation.
- A LDO is set separately for the power supply of the differential to single-ended part, isolating the power supply from the chip power supply.



Audio Input – DMIC

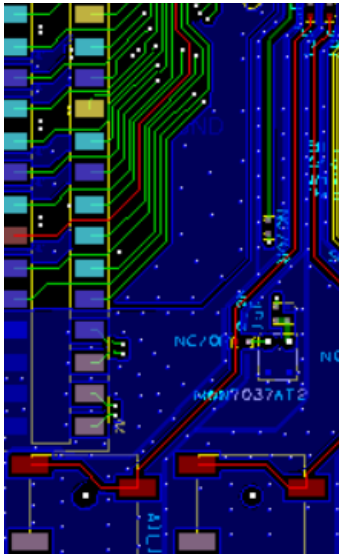
- Audio input path – DMIC:
  - Supports two digital microphone inputs.

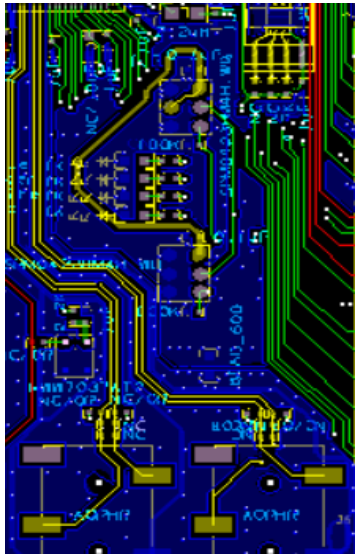




Audio – Layout Design

- Audio Input&Output:
  - Audio routing can't be parallel to the power line and high-speed signal lines, and as far away as possible, pay attention to crossover routing.
  - Audio alignment try not to change the layer over the hole.
  - Attention to the ground package treatment.





Change Logs

- 2023.03.20:
  - Initial version