Telink

# Telink Semiconductor

## TLSR827X Hardware Design Guideline

2024-09

# Scope

- Chip`s datasheet is the basic reference file of hardware design. This document will go through datasheet with hardware engineer and supplement some details. It will speed up projects after reading the document.
- Considering that the chip`s datasheet will be continuously updated, if there is any difference between this document and the chip`s datasheet, please refer to the latest version of the chip specifications.
- The version and link of the chip`s datasheet mentioned in this document are as follows:
  - DS -TLSR8278 -E_Datasheet for Telink BLE + IEEE802.15.4 Multi -Standard Wireless SoC TLSR8278( V1.0.4 )
  - http://wiki.telink-semi.cn/dokuwiki/doku.php?id=menu:chipset:tslr827x
- TLSR8258F1KET48 is taken as an example to describe. And the content mentioned in the file applies to the chipset as below:
  - TLSR8278
  - TLSR8273
  - TLSR8271
  - TLSR8355

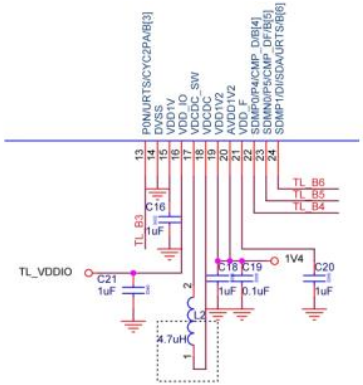
# Schematic Design Guideline

# Reference Schematic

- Reference Schematic:
  - Refer to chapter 20.
  - One reference design is listed here.
    - The reference schematic of TLSR8278F1KET48
    - BOM(Bill of Material)
  - The schematic is the design of minimum core system
    - Easy to copy into other designs.
    - Easy to count the cost at the stage of design-in.

# Pin layout

- Pin layout:
  - Refer to section1.6, then schematic and pcb footprint can be set up.
  - Power pins:
    - PIN15(VDD1V), internal digital core power supply. A decoupling capacitor, 1uF, is needed.
    - A serial 4.7uH inductor is **optional** connected between the PIN17(VDCDC_SW) and PIN18(VDCDC) as below figure shown.
    - PIN19(VDD1V2), internal DCDC power supply, route to PIN20 & PIN41(AVDD1V2), internal RF power supply.
    - PIN21(VDD_F), internal flash power supply. A decoupling capacitor, 1uF, is needed.
    - PIN16(VDD_IO), PIN27(VDD3), external power source, 1.8V~3.6V.



# Pin layout(Cont.1)

- Pin layout:
  - RF pins:
    - PIN40(ANT) is RF port.
  - Crystal pins:
    - PIN33(XC2), PIN34(XC1) connect 24Mhz crystal.
  - Debug pin:
    - PIN9(SWS) should be connected to a test point which is used to download firmware.
    - A group UART pin should be connected to test points which is used to do BQB test.
      - Some BQB binary files have been prepared on WIKI.
      - http://wiki.telink-semi.cn/dokuwiki/doku.php?id=menu:tools:bqb

# Power Supply

- Power Supply:
  - Refer to chapter 19.2
  - Power-supply voltage: 1.8V~3.6V
    - When power supply voltage is 1.8V~3.6V (e.g. dual dray batteries are used to supply power), the power supply is directly connected to the chip.
    - When power supply voltage is lower than 1.8V (e.g. single dry battery is used to supply power), external boost DCDC is needed.
    - When power supply voltage exceeds 3.6V (e.g. lithium battery is used to supply power), external buck DCDC or LDO is needed.
- Decoupling capacitors:
  - Refer to chapter 20.1
- DC-DC inductor:
  - Refer to chapter 20.1
  - The recommended inductance for DCDC is 4.7uH.

# Power Supply (Cont.1)

- Description of the selection of DCDC inductor:
  - The smaller the inductance value is, the stronger the load-carrying capacity of DCDC is, but the power consumption will increase. So we took a compromise and recommended the configuration of 4.7uH, in order to meet the Audio, ADC,RF,DigCore and other modules work high performance at the same time.
  - To ensure the DCDC load capacity and DCDC efficiency, the requirements for DCDC inductance selection are as follows:

    Inductors of wire wound type, low DCR and high-rated current are required. It is prohibited to use laminated inductors with high DCR, low-rated current.

| Parameters | Recommended parameters | Reference model 1(SPH201610H100MT) | Reference model 2(WPN201610H100MT) |
|---|---|---|---|
| Type | Wire wound | Wire wound | Wire wound |
| DCR | <1Ω | 0.935±20% | 0.757±20% |
| Rate current | >450mA | 470 | 700 |

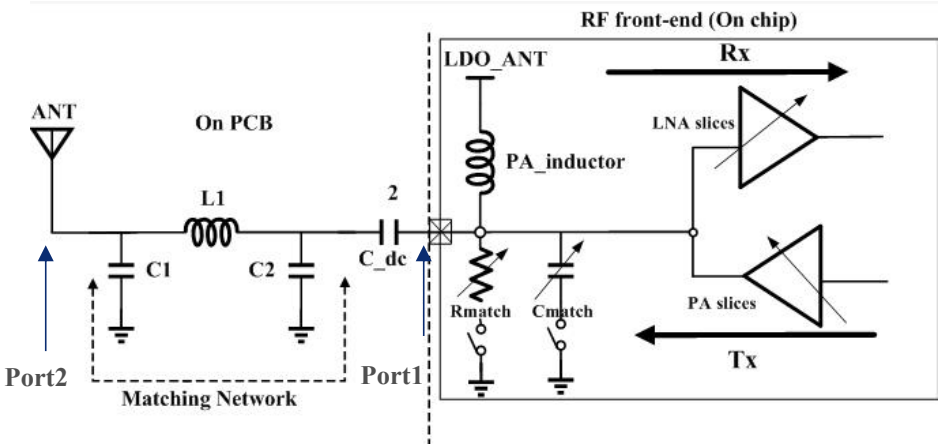
**Note: If the customer is unable to determine whether the selected inductors meet the specification requirements, he/she can consult the Telink FAE and use the Telink development board to measure the efficiency. It is recommended to use a wire wound inductor with an efficiency greater than 80%.**

# Power Supply (Cont.2)

- Description precautions of the embedded LDO/DCDC:
  - The chip embedded one 1.4V LDO/DCDC module and one 1.8V LDO/DCDC module. The default configuration in the SDK is 1.4V LDO and 1.8V LDO mode. For the specific power block diagram, refer to section 2.5
  - To meet different customer needs, explain the precautions for using 1.4V/1.8V LDO/DCDC:
    - Dual LDO mode, the ripple is small, the power response is fast, the power consumption is acceptable, it is recommended that the dual LDO mode is preferred, this mode is more stable.

    If there are certain requirements for power consumption, you can choose 1.4V DCDC+1.8V LDO mode.
    - Dual DCDC mode, the current will be smaller, but the ripple is larger, the power response will be slightly slower.
    - 1.4V DCDC+1.8V LDO mode, this mode can be selected when there are certain requirements for power consumption and the performance of audio and ADC.

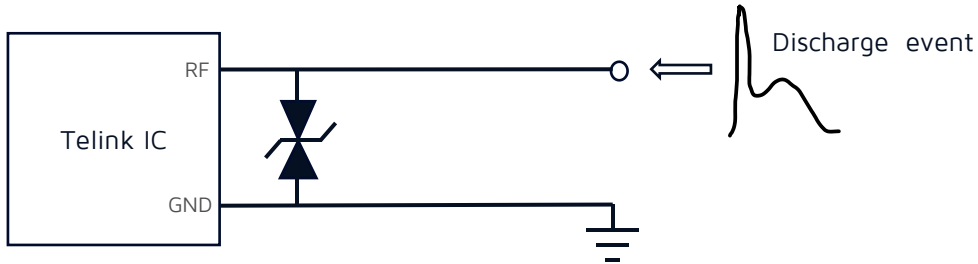
# RF front-end



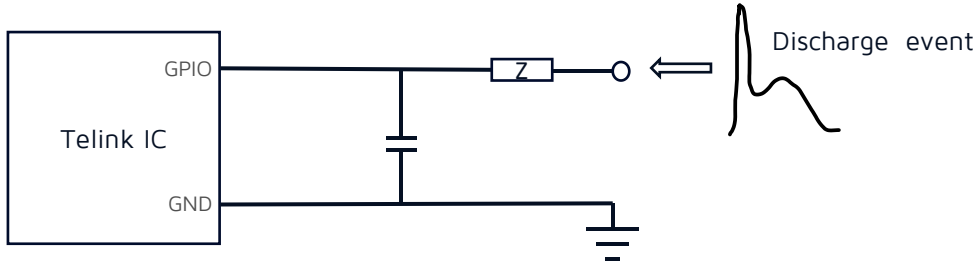

- Impedance seen from ANT towards chip should be 50ohm.(port2)
- Rx is disable when TX mode(port1 to LNA is high Z), also TX is disable when Rx mode.
- The impedance of TX from port1 to ANT is about 300ohm.
- When the impedance from ANT towards the chip is 50ohm, thus every point on the matching network will be a conjugate match, so the left and right sides of the dotted line will be conjugated impedance,. We get PA output impedance (on the right side of the dotted line) is 300+jX, so on the left side of the dotted line will be 300-jX.

# ESD protection

- If the product has high requirements for ESD protection, the TVS components are generally selected for the RF ports.The recommended model is TT0321SB/PESDRC2XP5VB.
  - The TVS component is in a high impedance state by default. When the discharge event occurs, it changes to a low impedance state, quickly releasing the current while clamping the voltage within the normal range.




- Resistor or LPF networks can be used for ESD protection of low-speed signals.
  - It can effectively reduce the voltage and current through the GPIO port.



# Certification

- Cdc (default value: 220pF) is connected to the ANT pin. If the capacitor is not connected, and test instrument can not block DC signal, test may be abnormal.
- C1, L1, C2 are used for circuit matching during certification, the values of which are flexibly adjustable corresponding to layout.
- Firstly, use VNA (Vector Network Analyzer) to do RX matching.
  - Customers must power on DUT, and use EMI tool to configure 8278 into RX mode, then tune RX matching.
- After RX test is finished, SA (Spectrum Analyzer) should be used to check TX harmonic.
  - If harmonics do not meet the requirements, re-do RX matching.
    - Use the VNA to adjust component value to meet the impedance matching requirements, and then check TX harmonic again.
- **ATTENTION:**
  - **It is recommend to mount a shielding box on PCBA for certification if customer can afford the cost. It is easy to pass certification and save time.**

# Crystal

- Crystal:
  - Refer to section 19.4.
  - The recommended specifications are as follows:
    - 24Mhz – 12pF - +/-20ppm
  - The range of internal load capacitor is among 5pF~18pF.
  - Internal load capacitor is suggested in application.
- RTC crystal:
  - Refer to section 19.4& 20.1
  - PC2 and PC3 can be used to connect external 32.768Khz crystal.
  - The recommended specifications are as follows:
    - 32Khz – 9pF - +/-20ppm

# Interface

- GPIO:
  - Refer to section 7.1.
  - All GPIO pins can be  configured to pull-up resistor and pull-down resistor.
  - All GPIO pins can be independently configured as high-level/low-level wakeup source.
  - When PA5(DM) is at high level and PA6(DP) is in floating state and using burning EVK tool to burn/debug the blank chip through SWS, it will randomly fail to communicate
    - It is recommended not to pull PA5 (DM) high in hardware design as default, such as connecting  this pin to VCC through LED.

- PWM:
  - Refer to chapter 8.
  - Up to 6 PWM output channels. Each PWMx(x=0~5) has its corresponding inverted output pins, PWMxN.
  - PWM0 pins, including PWM0 and PWM0N, can be used as IR driver pin.

# Interface(Cont.1)

- AMIC:
  - Refer to section 1.6 and 9.1.2.1.
  - AMIC (Analog MIC) adopts single-ended input
  - PC1 can be configured as AMIC single-ended input, other GPIOs can be configured as AmicBias.

- DMIC:
  - Refer to section 1.6 and 9.1.2.2
  - One group DMIC pins, PA1 and PA0.
- I2S:
  - Refer to section 1.6 and 9.1.2.3.
  - Support one group I2S pins, PD7,PA1, PD2,PD3 and PD4.
- SDM:
  - Refer to section 1.6.
  - Support two groups of SDMP/SDMN output pins, PB4/PB5 (SDMP0/SDMN0), and PB6/PB7 (SDMP1/SDMN1)

# Interface(Cont.2)

- UART:
  - Refer to section1.6 and 7.5.
  - Supports general UART interface and 7816 UART interface. General UART and 7816 UART share the same hardware circuit. General UART supports full-duplex transmission and reception, but 7816 UART only supports half-duplex as per 7816 spec.
  - Only Baseband, AES, UART/IR support DMA. UART and IR share the same DMA channel.
  - Any TX and RX can be configured into a group to use.
  - 7816 UART pins, including PD7, PC2, PD0 and PD3, can be configured as 7816 UART function or general UART UTX function, but DO NOT support UART URX function.
  - 8278 only has one set of UART hardware circuit.
  - Detail info:
    - TX pins: PA2, PB1, PC2,PD0,PD3,PD7
    - RX pins: PA0, PB0, PB7, PC3, PC5, PD6
    - Baud rate: 300/600/1200/2400/4800/19600/14400/38400/56000/57600/115200

# Interface(Cont.3)

- I2C:
  - Refer to section 1.6 and 7.3.
  - PC0/PC1, PC2/PC3, PA3/PA4 and PB6/PD7 can be configured as I2C master/slave mode.
  - For supporting up to 400K bit/s, external pull-up resistors must be added.
  - 8278 only has one set of I2C hardware circuit.
- SPI:
  - Refer to section 1.6 and 7.4.
  - PA2/PA3/PA4/PD6 and PB7/PB6/PD7/PD2 can be configured as SPI function and support both maser and slave mode.
  - 8278 only has one set of SPI hardware circuit.
  - 8278 supports 500Kbps, 1Mbps, 2Mbps, 4Mbps.
- SPI and I2C can be multi-used as below.
    - I2C and SPI cannot be used as Slave mode at the same time.
    - I2C Slave and SPI Master mode can be used at the same time.
    - I2C Master and SPI Slave mode can be used at the same time.
    - I2C and SPI can be used as Master mode at the same time.

# Interface(Cont4)

- ADC:
  - Refer to chapter 1.6 and 12.
  - Supports up to 10 detect pins, including PB0~PB7, PC4~PC5.
- Battery voltage detect:
  - When power supply voltage is lower than 1.8V (e.g. single dry battery is used to supply power), external boost DCDC is needed. Supply voltage should be sent to any ADC input channel for voltage detection.
  - When power supply voltage exceeds 3.6V (e.g. lithium battery is used to supply power), external buck DCDC or LDO is needed. User should implement voltage division to the supply voltage, so that it's decreased below 3.6V. Then this voltage lower than 3.6V should be sent to any ADC input channel for voltage detection. Each ADC input pin has embedded voltage divider circuit.
  - When power supply voltage is 1.8V~3.6V (e.g. dual dray batteries are used to supply power), user does not need to directly connect the power supply to ADC input channel.

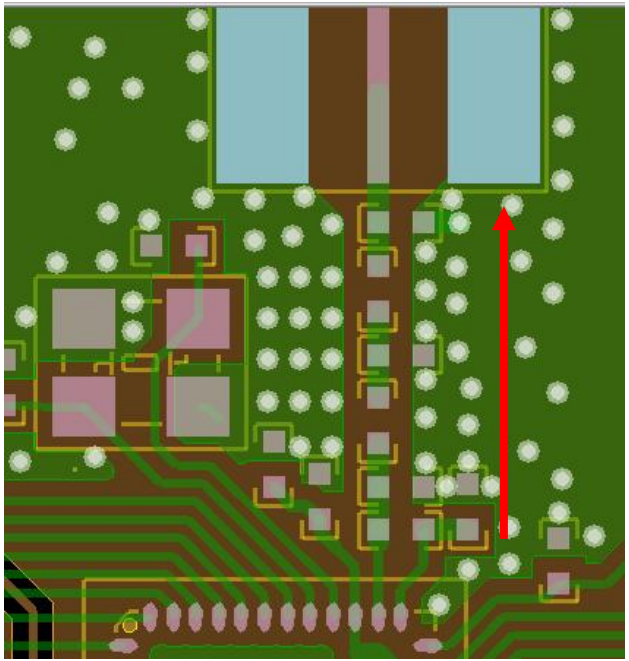
# Interface(Cont.5)

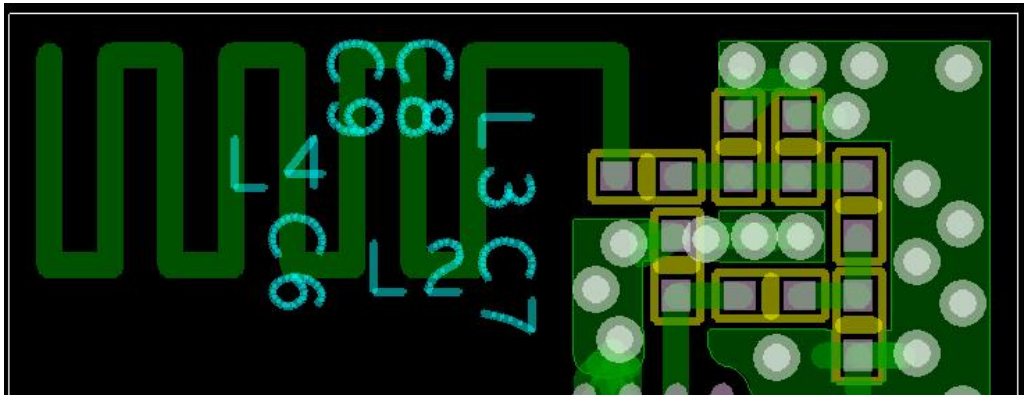
- External RF front-end pins:
  - Refer to section 1.6.
  - TXCYC is used to control the PA (Power Amplifier) of external RF Front-end: PB3, PC7, PD1.
  - RXCYC is used to control the LNA of external RF Front-end: PB2, PC6, PD0.
- Antenna Select pins:
  - Refer to section 1.6.
  - Two groups of SEL<0:2>: PD6/PB0/PB1, PC5/PC6/PC7. SEL<0:2> are used to select one of up to eight external antennas. The selected antenna channel is connected to the RF_IO pin.

# PCB Design Guideline

# RF layout

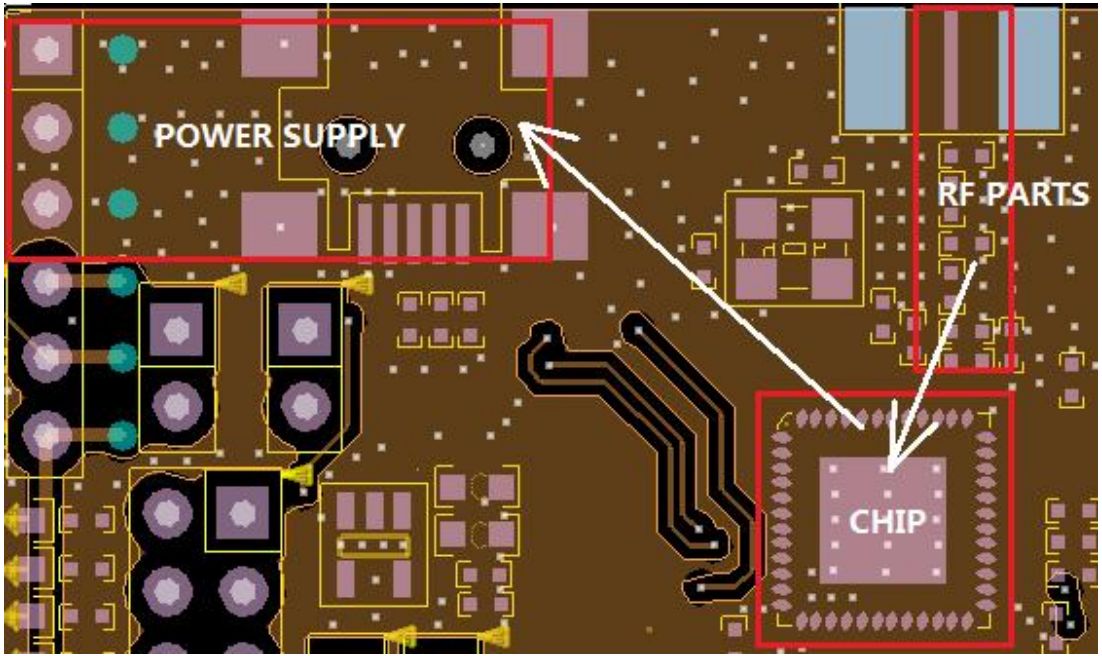
- The components on the RF path MUST be placed one by one. and they MUST be placed close to each other, no stub.
- It the area is not enough, can fold it, but MUST use ground and via to shield RF trace.

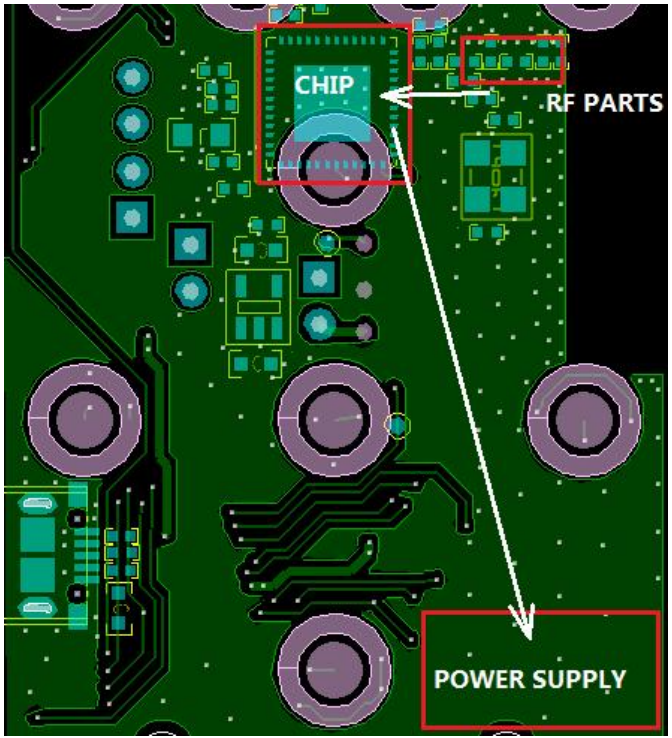




# Solid Ground Plane

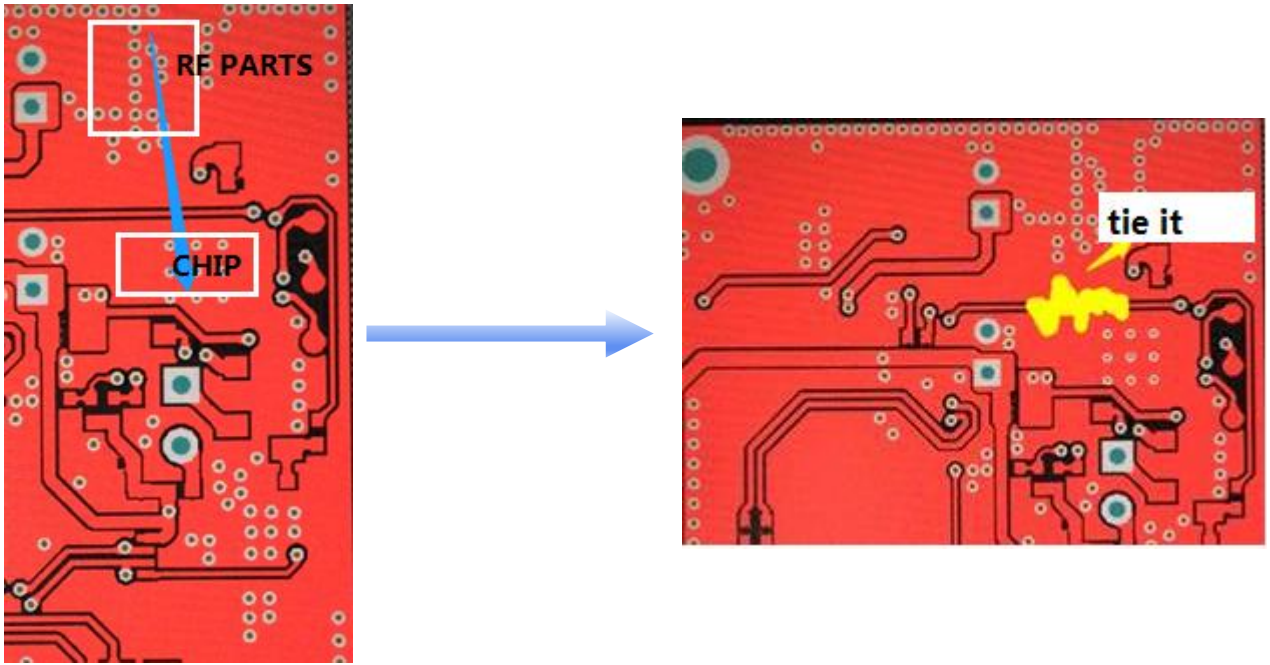
- The ground plane MUST be wide, solid. The ground plane from power supply to chip, then at last to RF parts MUST be solid.
- A good examples are as below.



# Solid Ground Plane(Cont)

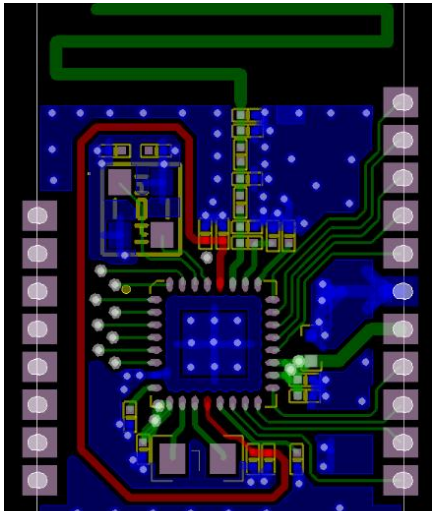
- A bad example is as below.
  - Ground plane between RF parts and chip is cut off, the rx performance is greatly affected.
  - Tie them together, the RX performance matches the data on the datasheet.



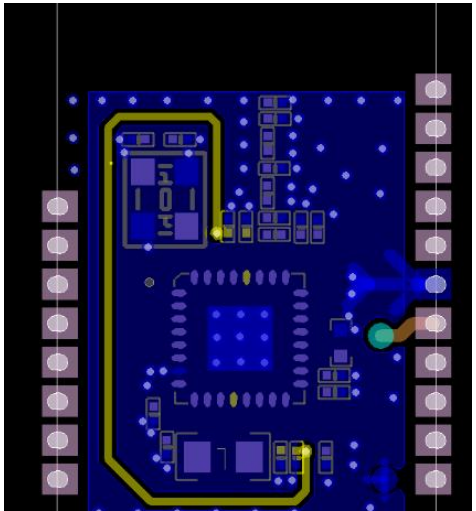
# AVDD1V2 Routing RULE

- AVDD1V2 is RF power supply, and its routing ways on PCB will have a great influence on RF;
- AVDD1V2 routing rules:
  - The trace must be as far away from the MCU as possible, but it also needs to be avoided from being too long;
  - The following figure is used as a reference according to the rule;

**First recommendation**

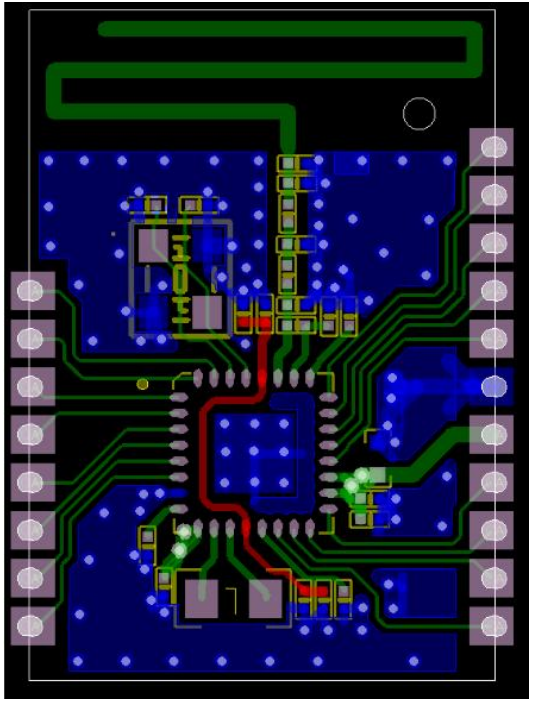


**Second recommendation**



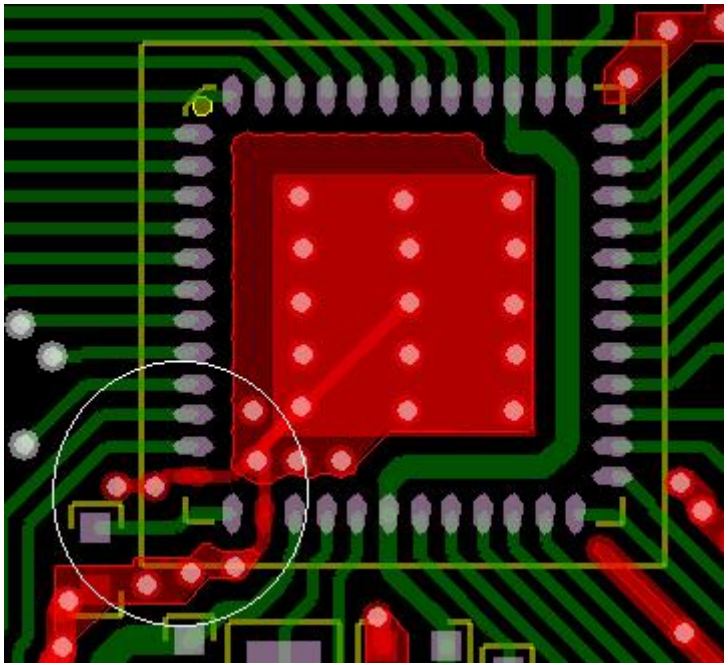
# AVDD1V2 Routing RULE(Cont)

- The following figure shows the bad routing;



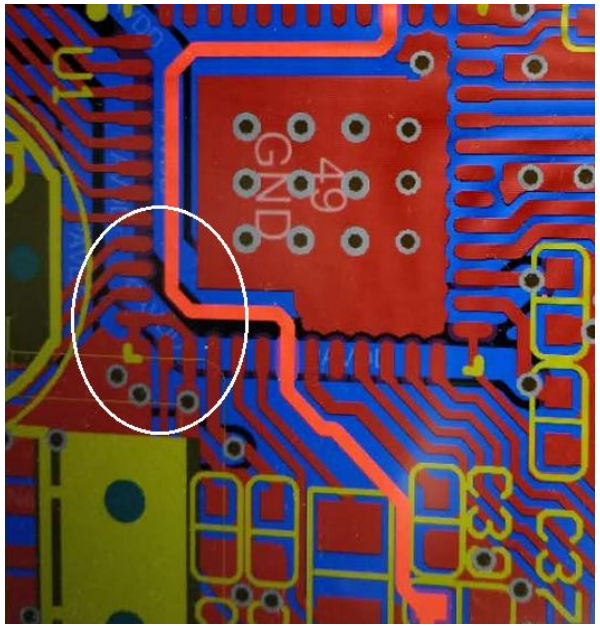
# VSS PIN

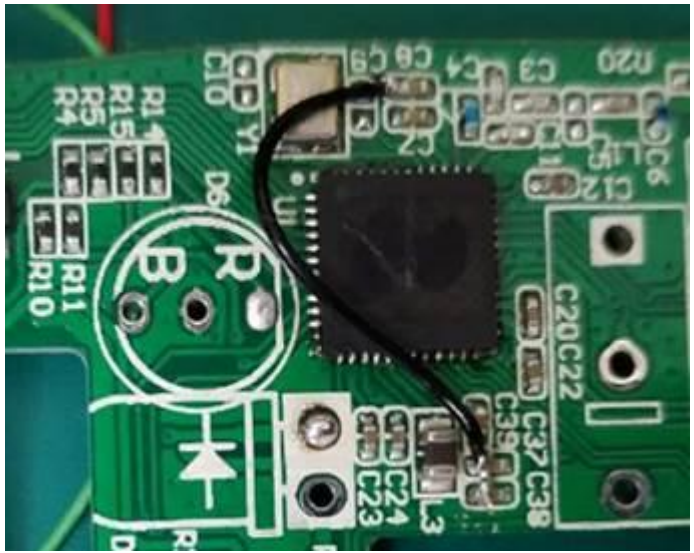
- VSS pins MUST be connected to the exposed pad.
- A good example is as below.



# VSS PIN(Cont)

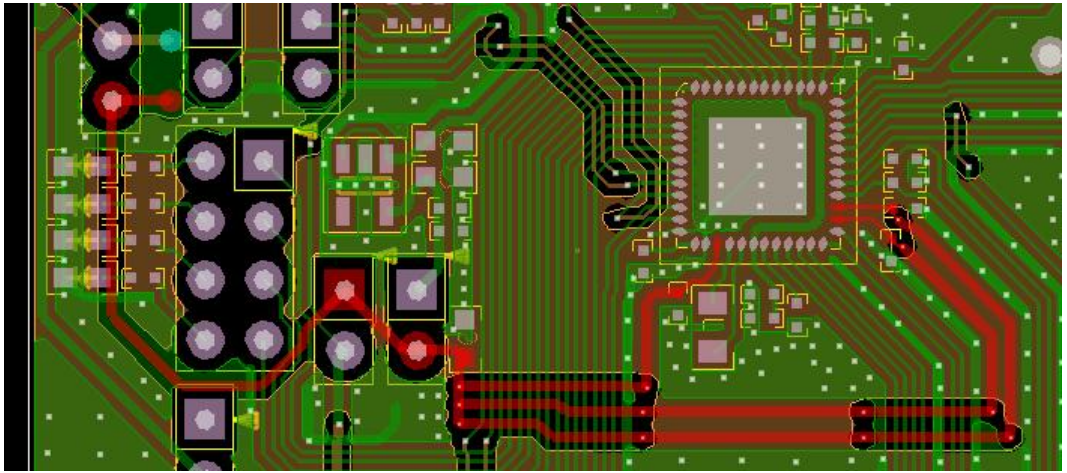
- A bad example is as below.
  - VSS pins are not tied to the exposed pad directly, the RX performance is greatly affected.
  - Re-working it, the RX performance matches the data on the datasheet.

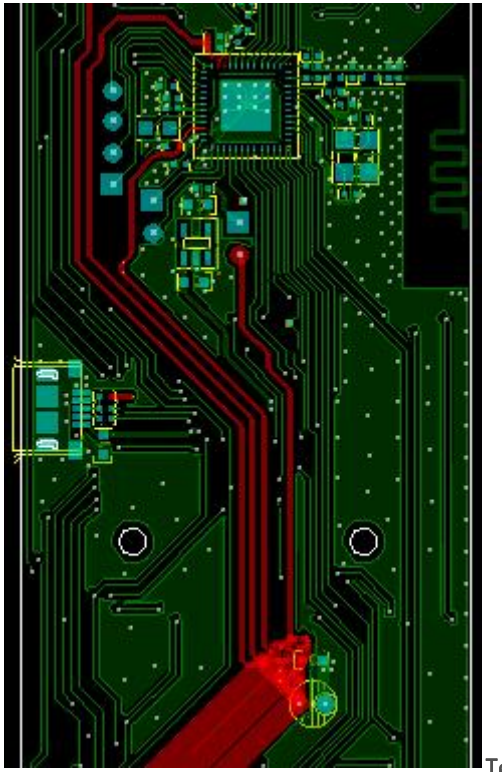


# Star connection

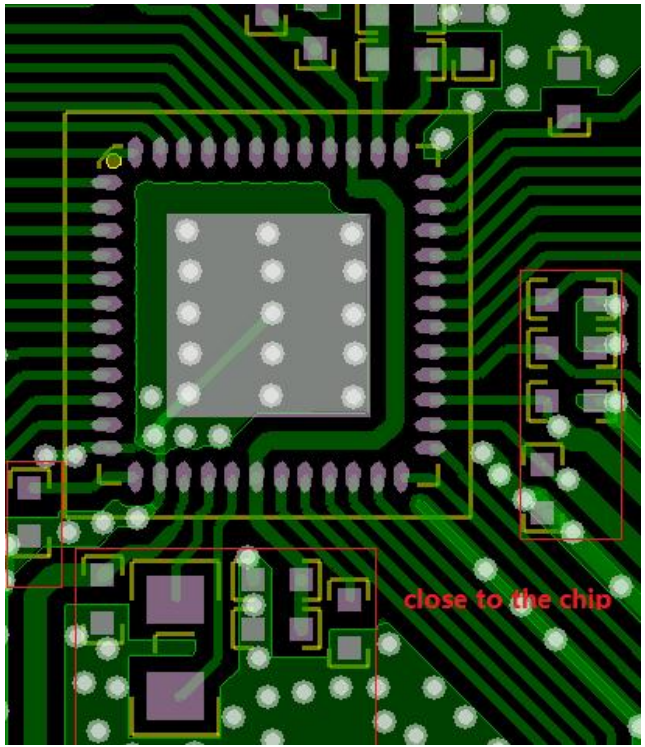
- Power supply should be connected in star-type connection.
  - If there is no audio function, can connect them together.

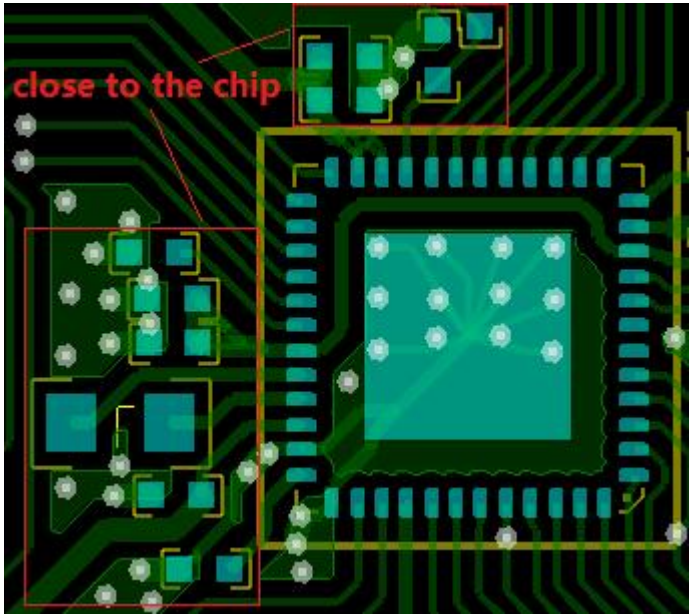




# Decoupling capacitor

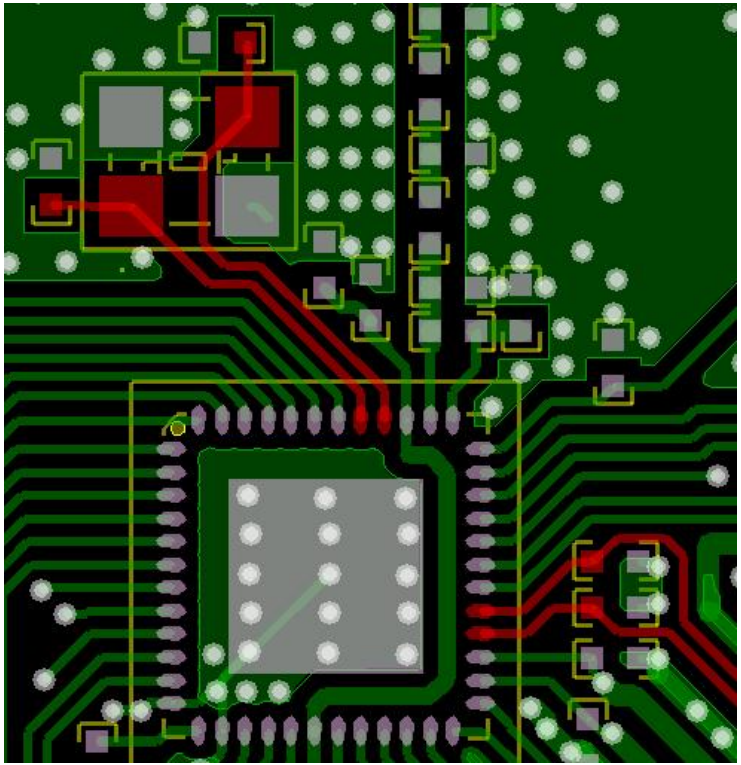
- Decoupling capacitors MUST be placed close to power pins.

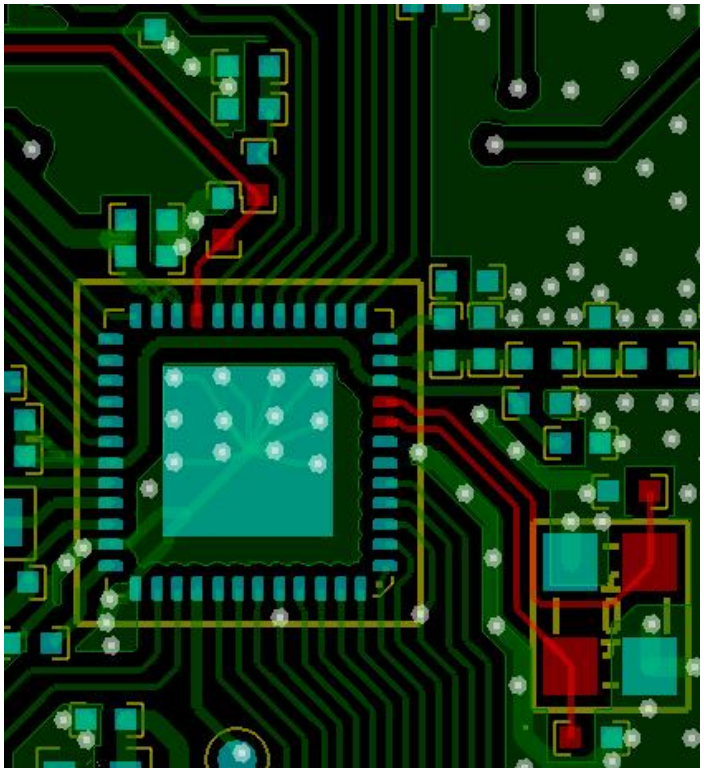


# Key traces

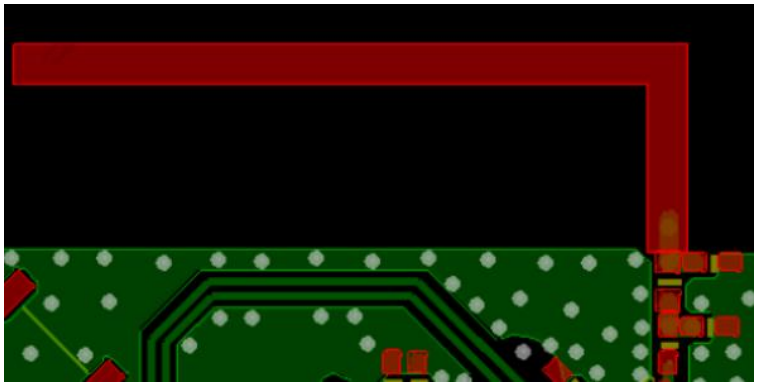
- To avoid EMI issue, some important parts such as crystal, audio trace, mic trace and usb trace MUST be shielded by GND and via.





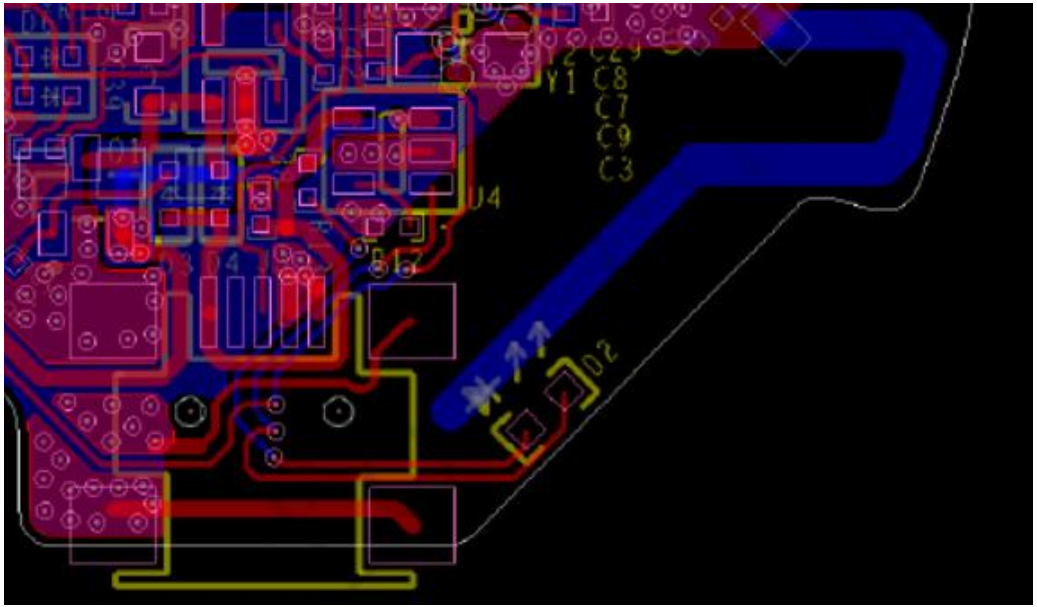
# Antenna – common requirement

- Antenna trace width shouldn`t be too narrow in order to decrease loss.
- Line width should be 0.5mm or above, generally it`s recommended to be 0.5mm or 1mm.
- Top and bottom of antenna location should not be covered by GND.
- The distance between antenna and GND should be 3mm or above.
- Generally antenna length is 20mm~30mm. The smaller the GND is, the longer the antenna should be.



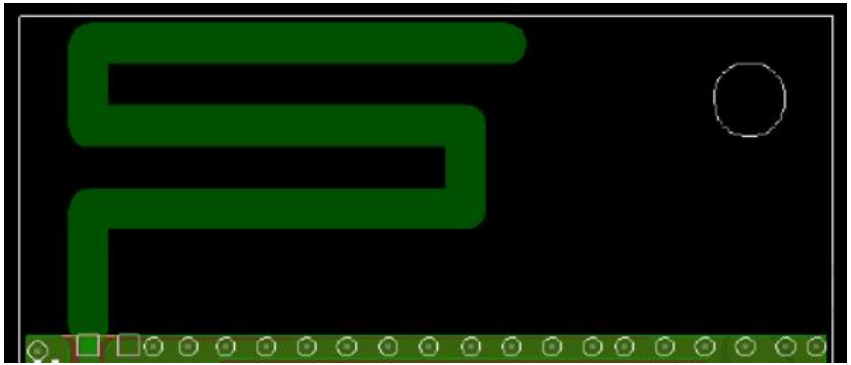
# Antenna – keep away others

- Keep PCB antenna far away from metal, battery, or other components, such as 3mm or 5mm.
- A bad example is showed as below. The antenna is too close to USB connector.



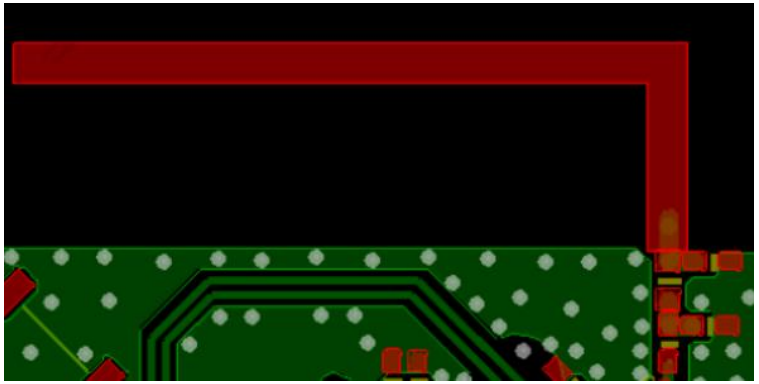
# Antenna – don`t exposed to others

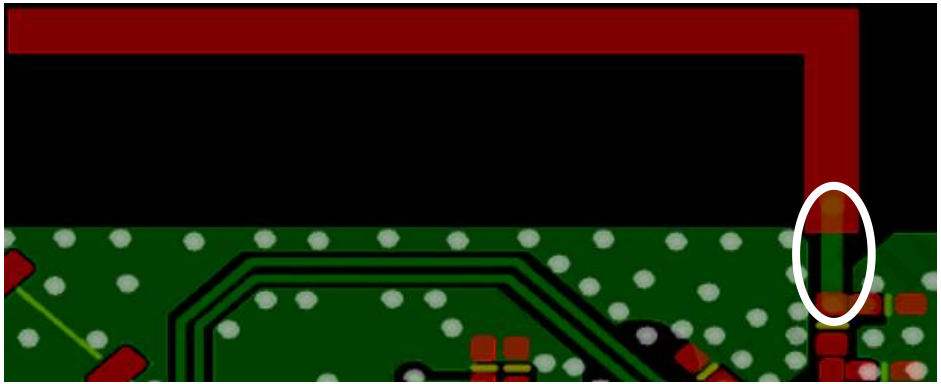
- There MUST be a row of via holes along the antenna on the side parallel to GND. Do not directly expose trace or pad to the antenna.
- The left is a good example. The right is a bad example.



# Antenna – matching components

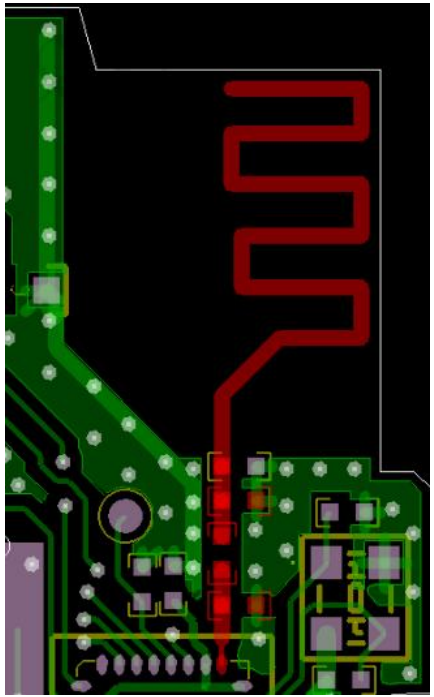
- Antenna matching components should be placed at the boundary of antenna and GND without shrink inward or expand outward.
- The left is a good example. The right is a bad example.

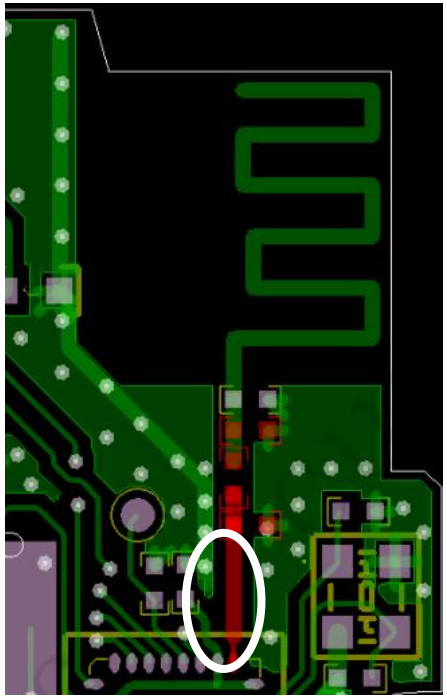




# Antenna – impedance design

- The RF line to the antenna port should be short. If RF trace can`t be designed shortly, it must be designed as 50ohm micro-strip line.
- The left is a good example. The right is a bad example.





# Change Logs

- 2020.04.07
  - Initial version
- 2020.04.17
  - Introduce how to design RF supply trace.
  - Shielding box is suggested.
- 2022.08.14
  - Added description to GPIO interface section
- 2023.01.04
  - Added description of the selection of DCDC inductor
- 2023.10.09
  - Added description of the embedded DCDC or LDO
- 2024.09.20
  - Adjust the range of internal load capacitor value.