Application Note：
Telink Generic FSK LL Introduction

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Brief：

This document is the brief introduction for Telink Generic FSK (Frequency Shift Keying) LL (Link Layer).

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Revision History

Version	Major Changes	Date	Author
1.0.0	Initial release	2019/4	QP, ZJ, ZFP, Cynthia

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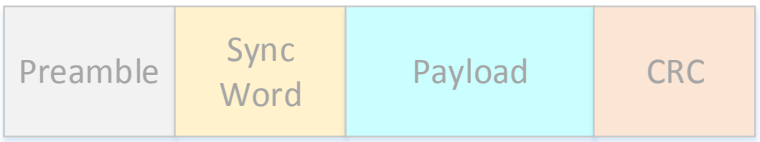

Figure 1 Format for fixed-length payload packet

Figure 2 Format for variable-length payload packet

Telink Generic FSK (Frequency Shift Keying) LL (Link Layer) supports two types of packet format, including:

- ✧ Fixed-length payload packet consisting of Preamble, Sync Word, Payload and CRC (Cyclic Redundancy Check).
- ✧ Variable-length payload packet consisting of Preamble, Sync Word, Header, Payload and CRC (Cyclic Redundancy Check).

1.1 Preamble

The preamble pattern is 0x55 or 0xAA. The Sync Word, which immediately follows the Preamble, determines the preamble pattern option to be selected by hardware: The controller hardware selects the preamble pattern based on the first transmitted bit of the Sync Word, so that the preamble's last bit is the inverted bit of the Sync Word's first bit.

The length of the preamble is programmable within the range of 0~31 octets.

***Note:**

Although the maximum allowable length can reach 31 octets, generally a typical application only requires 1~8 octets, while the extra octets are used for debugging.

1.2 Sync Word

In a network of associated devices, all devices generally share a common Sync Word.

A dedicated register is available to configure the length of the Sync Word within the range of 3~5 octets.

The Sync Word's content is also configurable via dedicated registers rather than the TX Packet Buffer.

Other third-party platforms may support at the same time more than one unique Sync Word of which any combination is searchable simultaneously. However, for Telink TLSR8258, only single Sync Word will be active at any time.

In addition, a register can be used to set the Sync Word match threshold. That is, during the PHY's Sync Word correlation procedure in RX mode, once the number of matched bits of the demodulated data reaches the pre-set threshold, the baseband will determine that an expected Sync Word has been synchronized.

In other words, the match threshold determines the maximum bit error tolerance for the PHY during Sync Word correlation.

Note that the received Sync Word is not stored in the RX Packet Buffer either. There is no dedicated status bit or interrupt signal to indicate the Sync Word matching, while the RX DONE irq may be taken as an alternative for that. Once the payload of a pre-set length has been received after a successful Sync Word matching, the RX DONE irq will be triggered regardless of the CRC result.

***Note:**

When the Sync Word match threshold is less than the length of the Sync Word (i.e. a bit error is allowed in the Sync Word), CRC computing will use payload and "correct" Sync Word, rather than actually received Sync Word passing the threshold but with error bit probably.

For example, for Sync Word of 0x11223344, received Sync Word could be 0x00223344 that passes the threshold. However, CRC computing will use 0x11223344 instead of 0x00223344. That means even though the Sync Word match threshold is less than the length of the Sync Word, the CRC still can recognize the possible bit error in the payload field.

1.3 Header

Only the packet format of variable-length payload contains the 9-bit Header field consisting of three subfields: 6-bit Payload Length, 2-bit PID, and 1-bit NO_ACK.

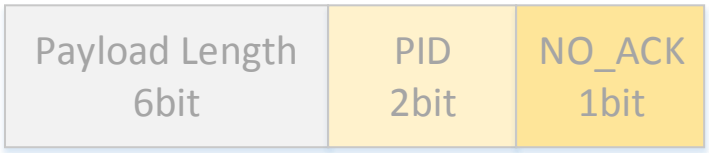

Figure 3 Header field

1) Payload Length

This subfield indicates the length of the payload in octet.

2) PID

This subfield is negligible for Telink Generic FSK LL, and it's reserved for Telink Primary TX/RX Link Layer. Its content is controllable by the software.

3) NO_ACK

This subfield is negligible for Telink Generic FSK LL, and it's reserved for Telink Primary TX/RX Link Layer. Its content is controllable by the software.

1.4 Payload

For the fixed-length payload packet, the Payload field directly follows the Sync Word, while for the variable-length payload packet, the Payload follows the Header field.

During transmission, the Payload bytes are transmitted in sequence with the rule of MSBit (Most Significant Bit) of the LSByte (Least Significant Byte) first. During reception, the Payload bytes are received also with the rule of the LSByte MSBit first.

For both TX and RX, the DMA method is used to exchange payload between the Radio Transceiver and the Link Layer.

For TX, a dedicated TX Packet Buffer in SRAM, an array of unsigned char element type, must be defined with the format depending on the packet type.

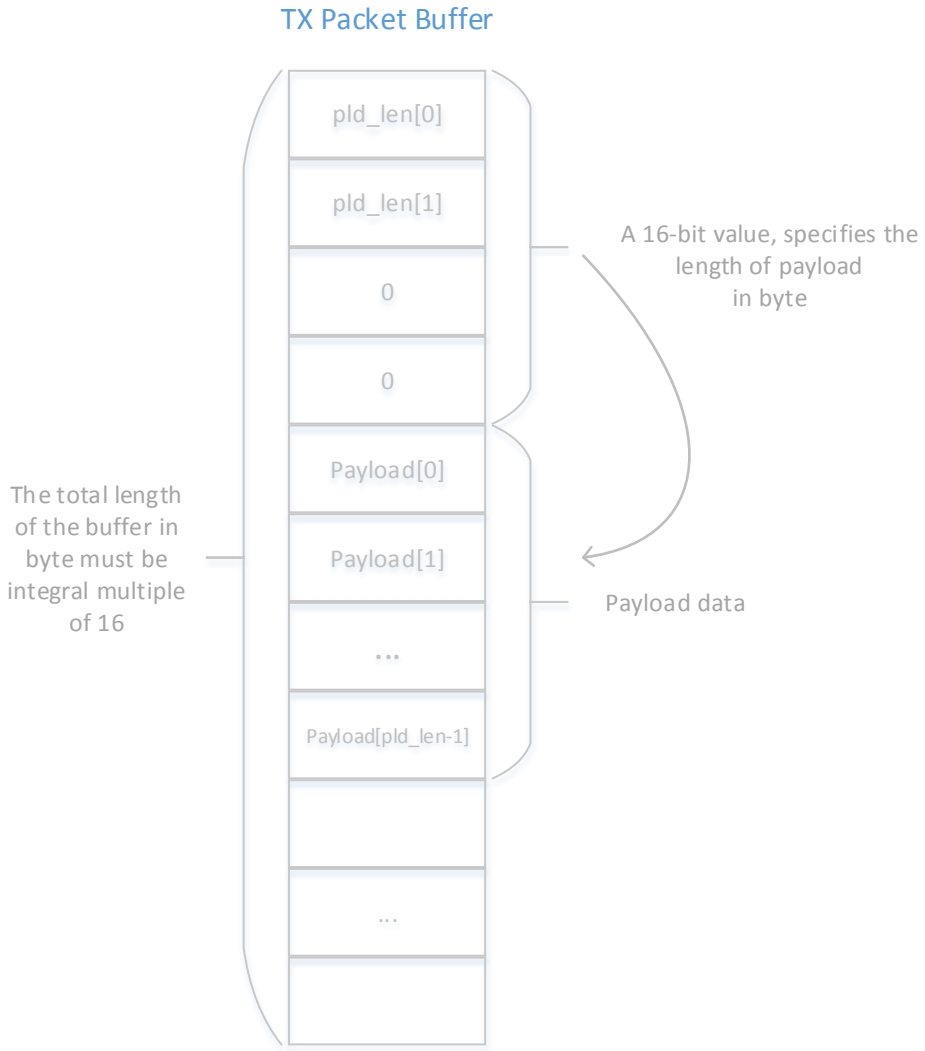

Figure 4 TX Packet Buffer for fixed-length payload packet

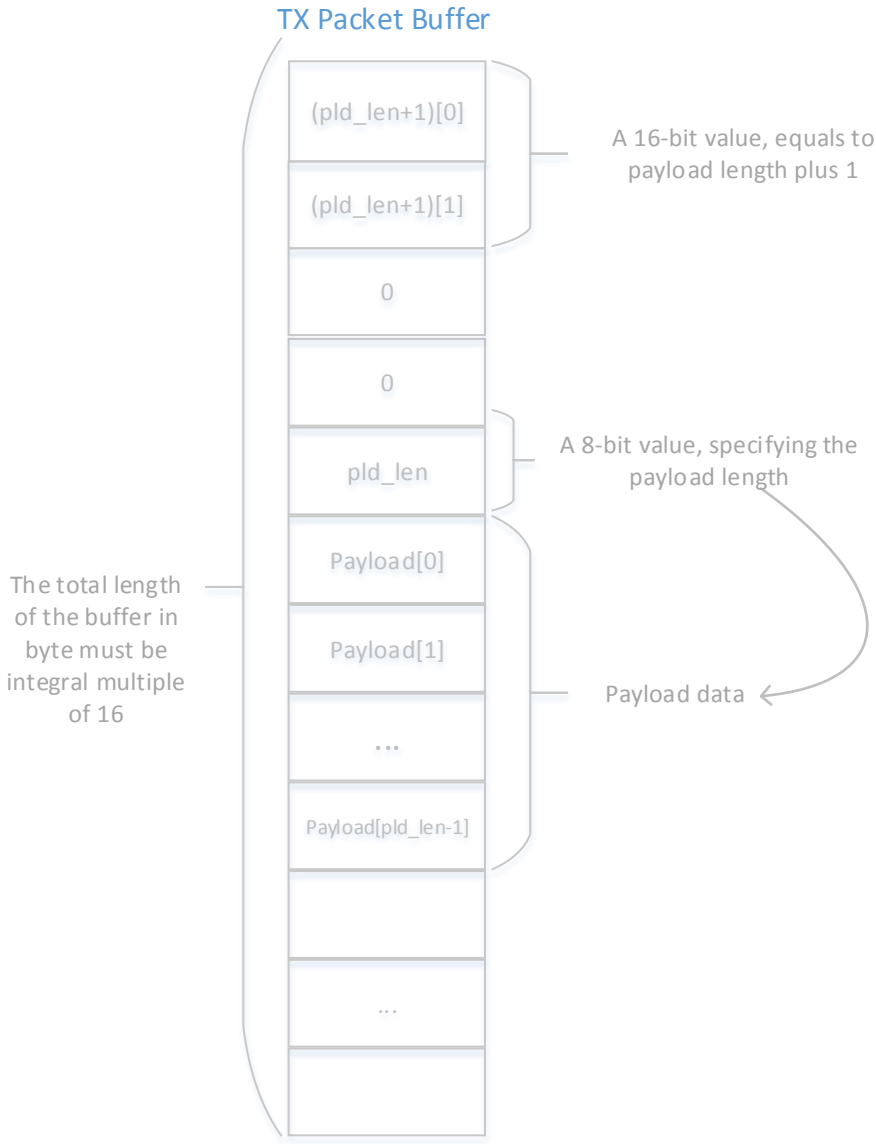

Figure 5 TX Packet Buffer for variable-length payload packet

Before starting the PHY's transmission, both the payload's length and the payload itself must be written into the TX Packet Buffer.

For RX, a dedicated RX Packet Buffer in SRAM, an array of unsigned char element type, must also be defined with the following format.

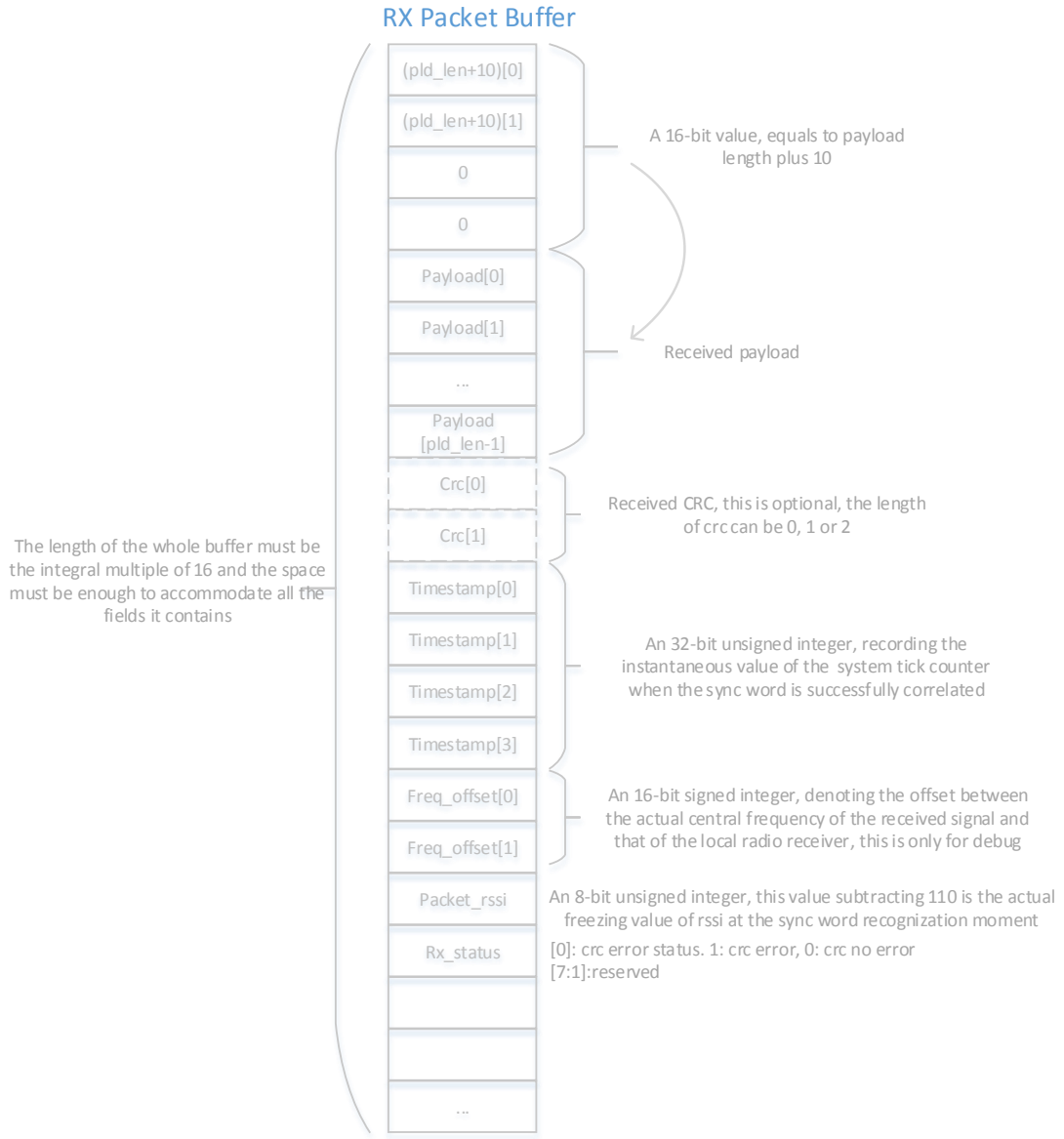

Figure 6 RX Buffer for fixed-length payload packet

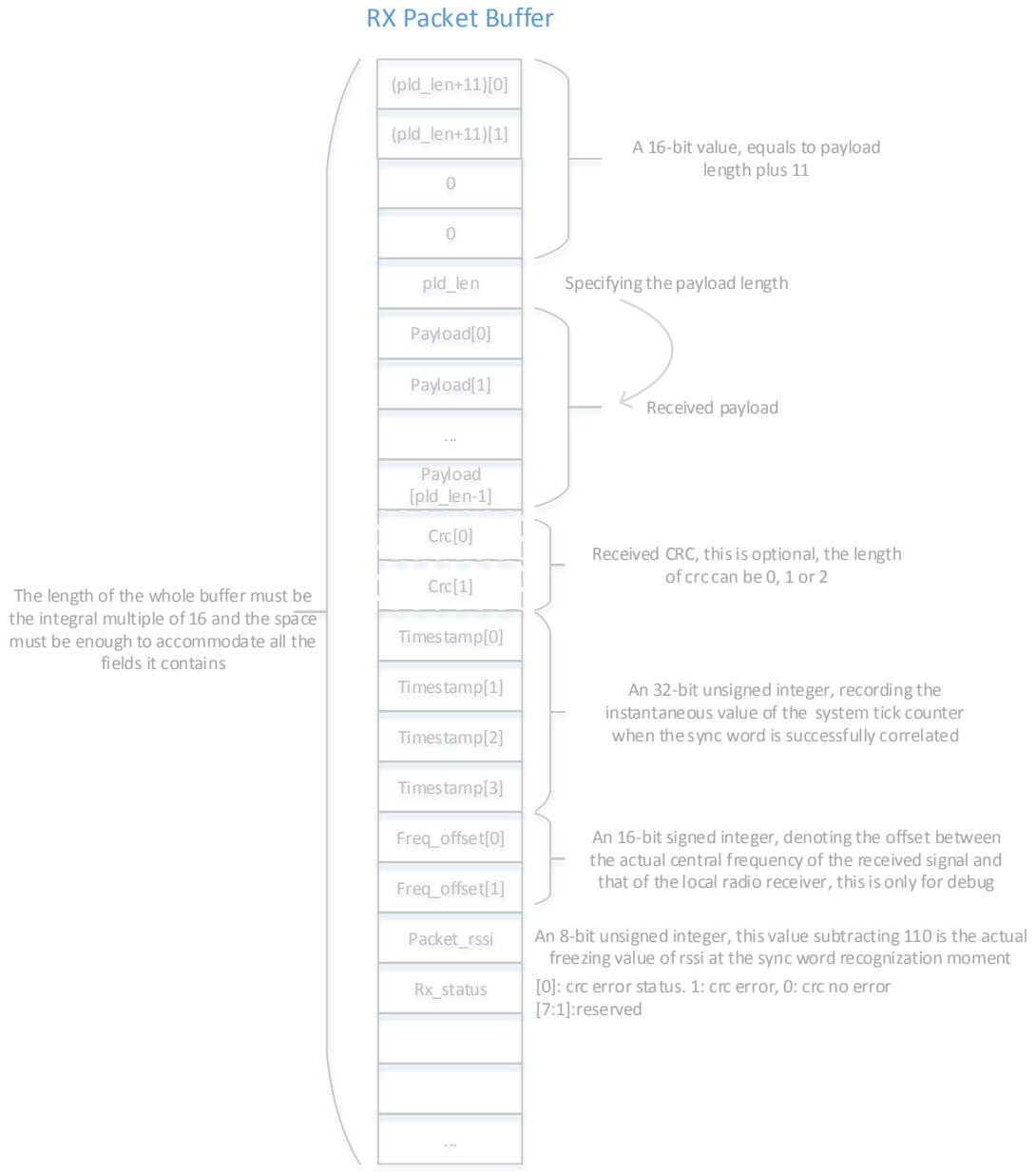

Figure 7 RX Buffer of variable-length payload packet

Notes:

1) For the fixed-length payload packet, before starting the PHY's receiver, a dedicated register should be used to pre-set an expected payload length. Once the Sync Word is successfully correlated, the Link Layer Controller will successively load the bytes of pre-set number, together with related RX information, into the RX Packet Buffer, and then generate the RX packet irq immediately.

2) For the variable-length payload packet, the Link Layer Controller determines the payload length according to the “Payload Length” subfield included in the Header field.

1.5 CRC

The CRC is a mechanism of error detection in the packet and it directly follows the Payload.

The portion of the packet over which to implement CRC calculation is programmable. For the TLSR8258, CRC is fixedly calculated over the Sync Word and the Payload.

The size of the CRC field is configurable within the valid range of 0~2 octets. “0” means CRC computing is disabled.

The polynomial and initial value of CRC LFSR (Linear Feedback Shift Register) are also fixed.

- ✧ The polynomial for 1-byte CRC is “X^8 + X^2 + X + 1”. Initial value is 0xff.
- ✧ The polynomial for 2-byte CRC is “X^16 + X^12 + X^5 + 1”. Initial value is 0Xffff.

2 Data Rate

Telink Generic FSK LL Controller provides a dedicated register to select bitrate as 2Mbps, 1Mbps, 500kbps or 250kbps.

3 Timebase

For Telink Generic FSK LL Controller, a 32-bit multi-purpose System Timer running at the rate of 16MHz can be employed to schedule all of its TX and RX activities, except during intervals of low power mode (suspend/deep sleep). The clock source is an external 24MHz crystal oscillator with high precision. The 32-bit System Timer running at 16MHz rolls over (wraps around) a circle for every 268.4 seconds or so. The System Timer tick count value can be read and changed at any time by using related API.

Two 32-bit timer-compare registers, T1_CMP and T2_CMP, are provided in the TLSR8258. When System Timer tick value reaches the T1_CMP's value, the link layer controller can automatically launch a transceiver operation. Similarly, once System Timer tick value reaches the T2_CMP's value, the link layer controller can automatically stop a transceiver operation.

Four automatic transceiver operation modes, implemented by respective hardware state machines, are provided for users' convenience: Single TX, Single RX, Single TX to RX, and Single RX to TX.

3.1 Single TX mode

In this mode, only the T1_CMP is involved. That is, the transmission of the prepared packet starts on a T1_CMP match.

A TX DONE irq will be triggered once the transmission is completed.

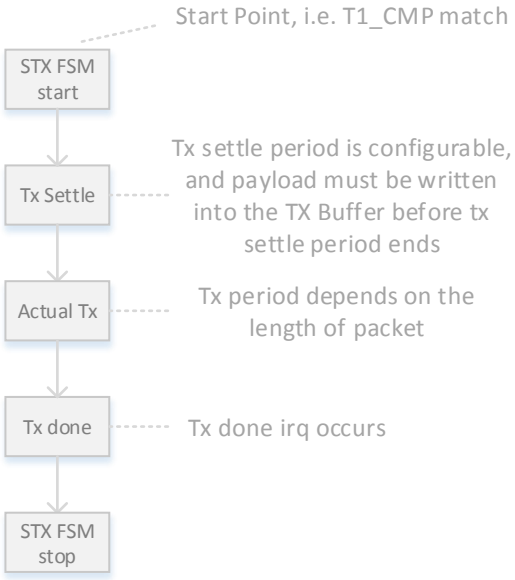

Figure 8 Timing sequence of Single TX

3.2 Single RX

In this mode, both the T1_CMP and the T2_CMP are involved.

When System Timer tick value reaches the T1_CMP's value, the transceiver enters RX state and starts to search for an expected Sync Word.

- ✧ If the sync word fails to be correlated until the System Timer tick value reaches the T2_CMP's value, a RX FIRST TIMEOUT irq will be triggered and the transceiver will return to IDLE state.
- ✧ If a packet is received before the T2_CMP match, a RX DONE irq will be triggered and the transceiver will return to IDLE state.
- ✧ It is also possible to disable the T2_CMP, so that the transceiver can always stay in the RX state until a packet is received.

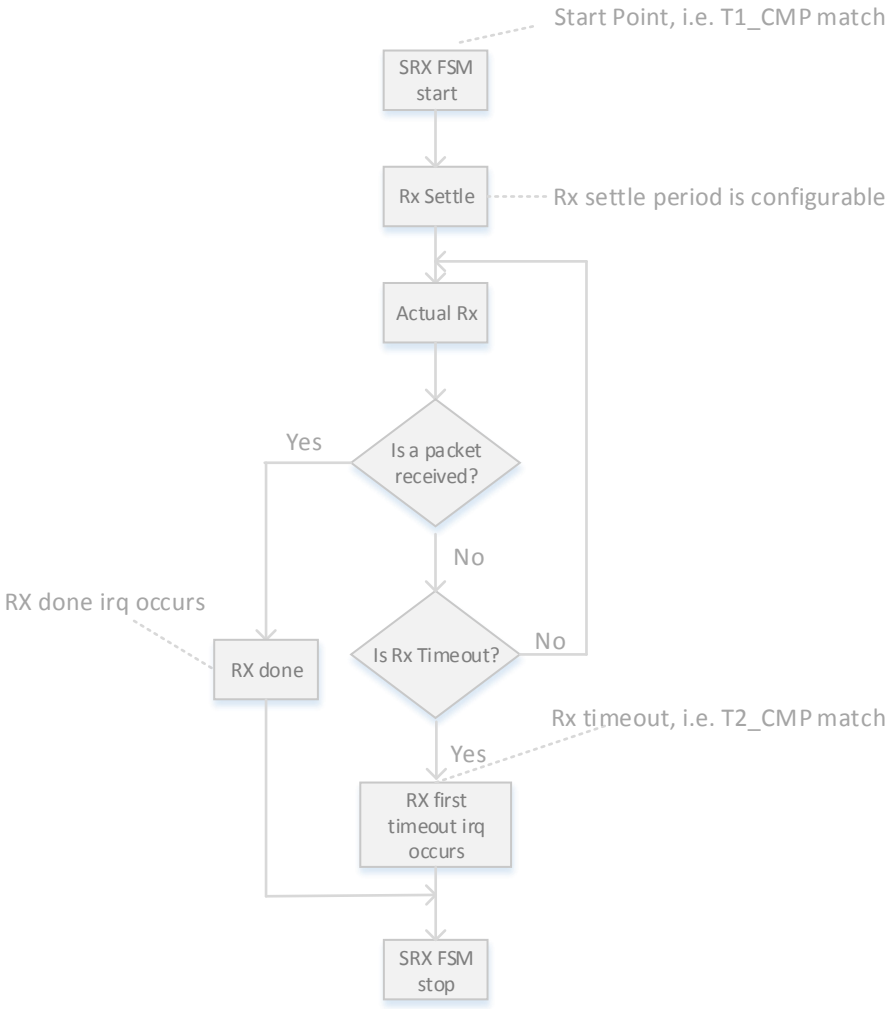

Figure 9 Timing sequence of Single RX

3.3 Single TX to RX

In this mode, both the two compare timers are involved. The transmission of the prepared packet starts on a T1_CMP match. And after the transmission is completed, a TX DONE irq is triggered, the transceiver waits for a short time (programmable), and then turns into RX state. If the sync word fails to be correlated until the System Timer tick value reaches the T2_CMP's value, a RX TIMEOUT irq will be triggered and the transceiver will return to IDLE state. If a packet is received before the T2_CMP match, a RX DONE irq will be triggered and the transceiver will return to IDLE state. This automatic mode applies to the scenario when an ACK or a response packet is desired after transmitting a packet.

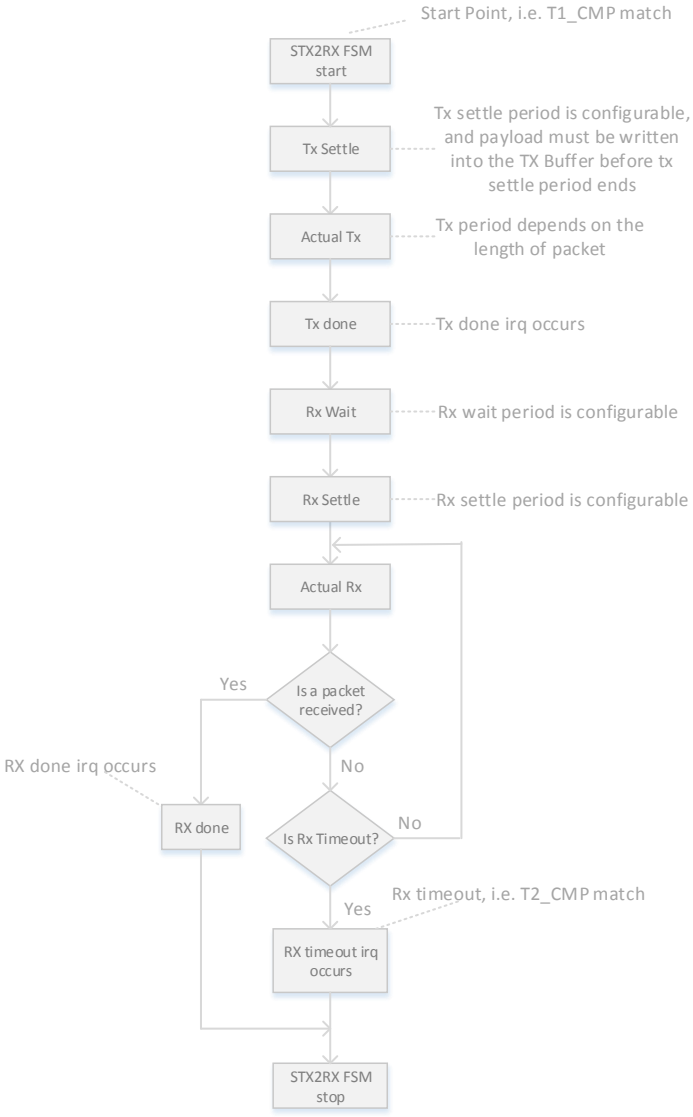

Figure 10 Timing sequence of Single TX to RX

3.4 Single RX to TX

In this mode, the transceiver enters RX state on the T1_CMP match and then waits for a packet reception. If no packet is received until the System Timer tick value reaches the T2_CMP's value, a RX FIRST TIMEOUT irq will be triggered and the transceiver will resume to IDLE state. If a packet is received before the T2_CMP match, a RX DONE irq will be triggered, and after waiting for a duration (programmable), the transceiver will turn into TX state and start the transmission of a prepared packet. This automatic mode applies to the scenario when it's needed to send an ACK or a response packet after receiving a packet.

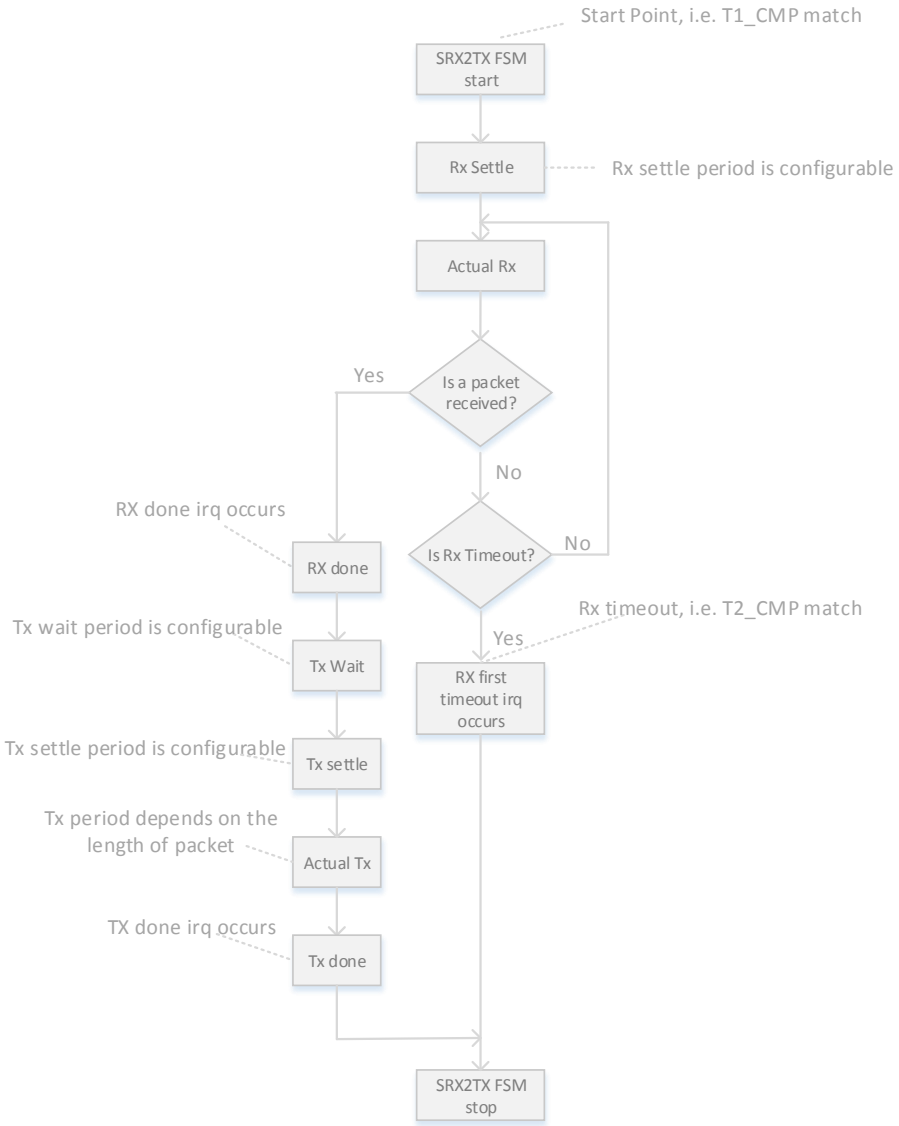

Figure 11 Timing sequence of Single RX to TX

4 Interrupt

There are totally four relevant interrupt signals for the Telink Generic FSK LL Controller: TX DONE, RX DONE, RX FIRST TIMEOUT, and RX TIMEOUT.

1) TX DONE

Once the transmission of a packet is finished, a TX DONE irq will be triggered.

2) RX DONE

Once a complete packet is received, as long as the Sync Word matches, a RX DONE irq will be triggered regardless of the CRC checking result.

3) RX FIRST TIMEOUT

In any of the two automatic modes (Single RX and Single RX to TX as described above), a RX FIRST TIMEOUT irq will be triggered when the T2_CMP matches.

4) RX TIMEOUT

Only in the Single TX to RX mode, will a RX TIMEOUT irq be triggered when the T2_CMP matches.

5 RSSI

There are two types of RSSI for the Telink Generic FSK LL.

- ✧ For the RX packet RSSI, which is stored in the RX Packet Buffer after a packet is received, its value equals to the actual freezing RSSI value at the sync word recognition moment plus 110.
- ✧ For the real time RSSI of a given channel, when the transceiver is in RX state at this channel, its value equals to a real time power measurement value of that channel read out from a dedicated register minus 110. The real time RSSI is usually used to check whether a given channel is busy.